AD-A152 987 LIQUID CRYSTAL MOS (METAL-OXIDE-SEMICONDUCTORS) MATRIX HIGH DENSITY PROGRAM(U) HUGHES AIRCRAFT CO CARLSBAD CA INDUSTRIAL PRODUCTS DIV W P BLEHA ET AL. 01 SEP 81 1/1

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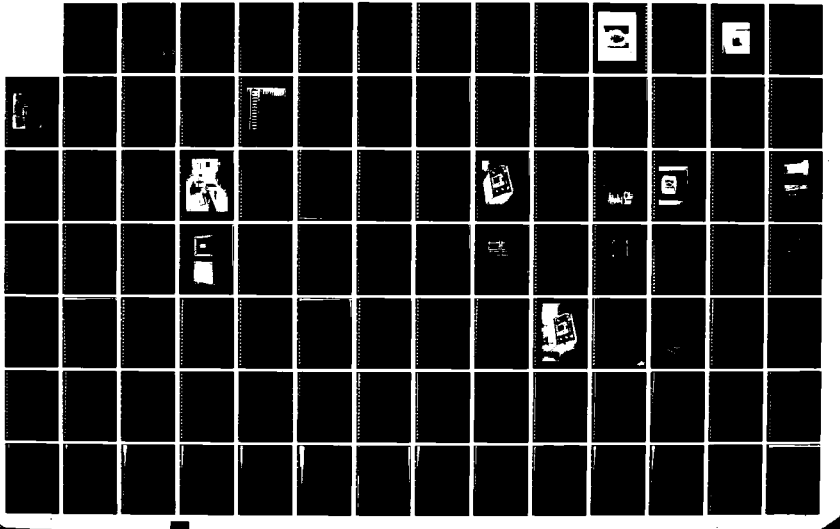

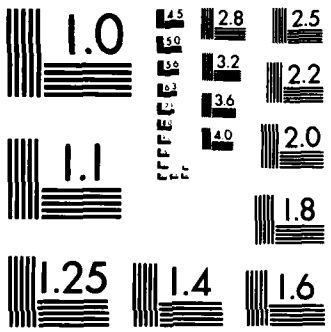

LIQUID CRYSTAL MOS MATRIX HIGH DENSITY PROGRAM

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1 September 1981
Final Technical Report for the Period 1 October 1978 to 1 June 1981

Unlimited Distribution

Prepared for:
United States Army
Mobility Equipment Research and Development Command
Night Vision and Electro-Optics Laboratory
Fort Belvoir, Virginia 22060

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* THE LIQUID CRYSTAL MOS MATRIX HIGH DENSITY PROGRAM		5. TYPE OF REPORT & PERIOD COVERED Final Technical Report 1 Oct 78 to 1 June 81 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) W.P. Bleha S.E. Shields R.B. Lloyd		8. CONTRACT OR GRANT NUMBER(s) DAAK70-78-C-0187
9. PERFORMING ORGANIZATION NAME AND ADDRESS Liquid Crystal Section, Industrial Products Division, Hughes Aircraft Company, 6155 El Camino Real, Carlsbad, CA 92008		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS U.S. Army Mobility Equipment Research and Development Command, Night Vision and Electro-Optics Laboratory, Fort Belvoir, VA 22060		12. REPORT DATE September 1, 1981 13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)*		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/ DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT *(of this Report)* 17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)* Unlimited Distribution		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)* Liquid Crystal Display, Flat Panel Display, Matrix Display, High Density Display, Helmet-Mounted Display, HUD Display, Weapon Sight Display		
20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)* Many of the requirements for tactical displays require that the display use little power, be compact and provide high resolution. MOS - addressed liquid crystal displays have been developed which address these requirements. In particular, a 240 x 320 element display, .75 inch x 1.00 inch in size has been developed during the course of work on this program. This display provides one quarter television resolution with greater than 6 grey shade capability. Several fully operational units have been delivered.		

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Higher density displays place more stringent requirements on the interconnect between the display and its drivers. One way to approach this problem is to integrate the display and its drivers into the same silicon substrate. Many facets of this integrated display and drivers concept have been successfully demonstrated on this program. These include the driver circuits themselves as well as the assembly and packaging of the integrated display.

FOREWORD

The completion of the Miniature Flat Panel Display program was the result of an interdisciplinary team effort by individuals from three separate areas of Hughes Aircraft Company. The Liquid Crystal Section of the Industrial Products Division was responsible for the overall program management, and the design, fabrication, and testing of the Liquid Crystal Matrix Display and its custom LSI drivers. The Display System Laboratory, Radar Systems Group, provided project and system engineering, and design staff for the electronic and mechanical tasks. The Electro-Chemistry section of the Hughes Corporate Research Laboratories formulated the liquid crystal material.

The team of individuals whose conscientious efforts contributed to the completion of the MFPD program included: Richart Bernstein, Bruce Fletcher, John Gunther, William C. Hoffman, Anna Lackner, Lew Lipton, J. David Margerum, Dave Murillo, Wilson Quan, Jim Rill, Warren Schnibbe, Craig Stephens and Andy Toth. The program was monitored and directed for the Army by James Brindle and David Bosserman. This report was typed by Eve Gonzales.

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1.0 INTRODUCTION

1.1 The LC/MOS Matrix Display Program

The purpose of this final technical report is to summarize the efforts and results on the high density (23.1 pixels per millimeter) display with integrated driver circuits (which is fully documented by the interim technical report); and to document the complete development effort on the medium pixel density active-matrix flat panel display (12.25 pixels per millimeter) which resulted from the redirection of this program. The medium density display, designated the H4080, has an array size of 240x320 pixels.

1.1.1 Scope

The scope of this effort involved the design, fabrication, demonstration, and delivery of a liquid crystal active-matrix flat panel display. The scope also included the development of mounting the metal-oxide- semiconductors (MOS) matrix display onto a suitable circuit board and the development of sealing techniques to achieve the required display operating performance. The initial program scope involved the development of the high pixel density liquid crystal matrix display; the program scope was redirected after twelve months of developmental effort to implementing the medium pixel density liquid crystal matrix display. A completed medium density display showing video imagery in the central 175x175 pixel area is shown in Figure 1-1.

1.1.2 Objective

The initial objective of this program was to demonstrate the feasibility for a high pixel density miniature flat panel display through the design, fabrication, and evaluation of a proof-of-progress breadboard and four feasibility models. The redirection of the program efforts changed the objective to demonstrating the feasibility for a medium pixel density miniature flat panel display. These latter displays were fabricated with the basic seven mask, MOS p-channel process sequence used to fabricate previous lower density displays.

1.1.3 Background

Hughes has demonstrated several active-matrix flat panel displays that have been made with low to high pixel densities, from a 3.94 to 23.1 pixels per millimeter (p/mm). Recent improvements in both the active-matrix display and the display-driver technologies have set the stage for this program to extend proven techniques and to fabricate a 240 by 312 pixel display matrix at a density of 23.1 pixels per millimeter (p/mm). This program progressed from the technology development achieved by fabricating a 23.1 p/mm Miniature Active Matrix liquid crystal video display, for the U.S. Army Mobility Equipment and Development Command under Contract Number DAAK70-77-0225. That program resulted in the demonstration of a defect-

Figure 1.1: H4080 Medium Density LC/MOS Display (240x320 pixels)
Showing Video Activa tion of 175 x 175 Pixel Array

free 100 by 100 pixel matrix (H4030 display) which allowed presentation of live video with full gray scale capability. This display met or exceeded all program requirements. A photograph of video on the H4030 display is shown in Figure 1-2.

A miniature CRT is presently used in magnified display systems used for Helmet Mounted Displays (HMD), Head-Up Displays (HUD), and Tank FLIRs. The major disadvantages of the CRT for these applications range from low life, low brightness, high voltage, and difficult maintenance actions in the HUD application to lack of ruggedness in the tank application. The development of a higher density matrix display would eliminate these disadvantages. The development of a higher density flat panel display would also provide the opportunity to develop much needed portable weapon mounted displays and hand-held target acquisition devices.

In order to extend the earlier development of the 23.1 p/mm high density display, it became evident that the most significant problem in the flat panel matrix display technology was the ability to interconnect the display to its drivers. After an evaluation of the technical problems and risks associated with various interconnect schemes, we concluded that the most desirable and least risky approach was to integrate the drivers directly with the display by using the same nine mask silicon processing techniques that were used in fabricating the 23.1 pixel per millimeter (p/mm) display (H4030).

Additional key technical challenges on the high density display program were the development of: (1) a stable high value resistor for assuring linear operation of the on-chip drive circuits; (2) a suitable light blocking layer for protection of the underlying transistors in the active display area; and (3) a compatible intermediate dielectric material for isolating the light block layer and smoothing the active display surface. Successful achievements in the first area were obtained by controlling the resistivity of a doped polysilicon layer to the tolerances required for the linear drive circuitry. However, after twelve months on this program, no acceptable solutions had been found for the light blocking and intermediate dielectric layers. As a result of these problems, an alternate technical direction for this program was established. The approach taken was to increase the pixel density to the maximum consistent with the well-established technology previously developed. This was determined to be a pixel density of 12.3 p/mm instead of 23.1 p/mm. In addition a display size of 240 x 320 pixels was chosen, similar to the high density display goal. This allowed for 4 displays to be placed on one three-inch-diameter wafer to improve display yield.
Finally the existing drivers, interfacing to the display with flexible cables, would be utilized in the electronic demonstration models.

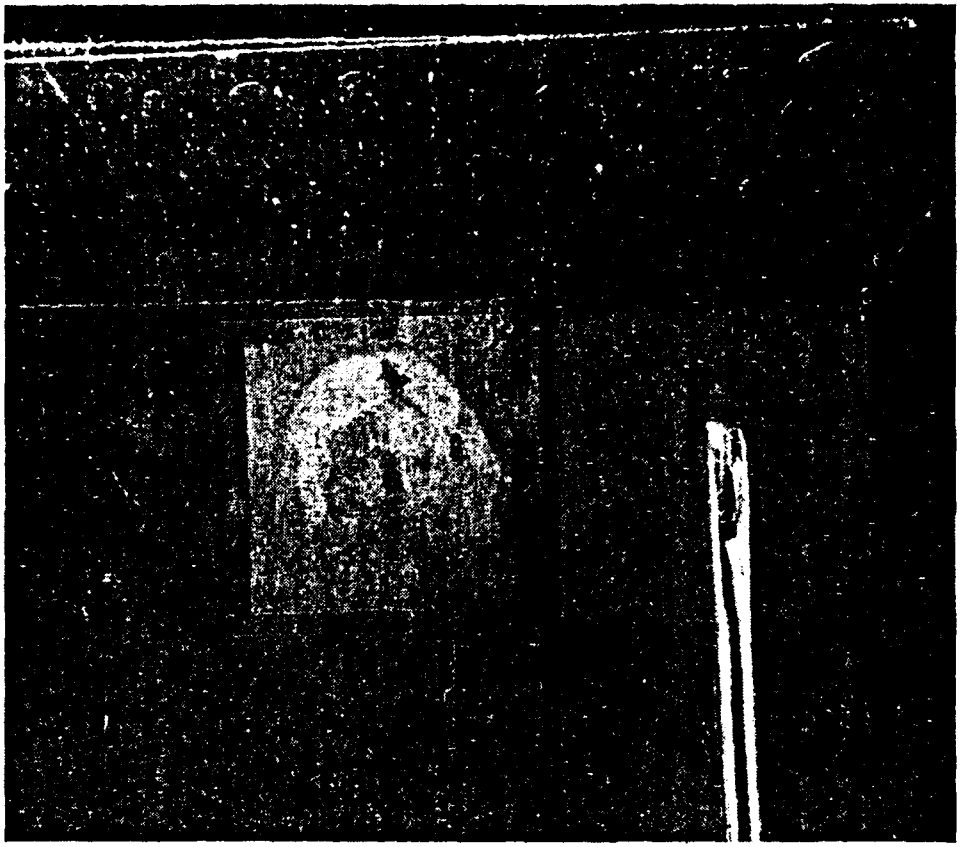


Figure 1.2 Minature Active Matrix (H4030) Display with Video

Further development of this display would result in a hybrid package with drivers mounted on the periphery of the active area. This package would then serve as a common optical module for displays requiring higher pixel counts. For example, four modules could be optically combined, yielding a 480 x 640 pixel image source for the projection Heads Up Display (HUD) unit.

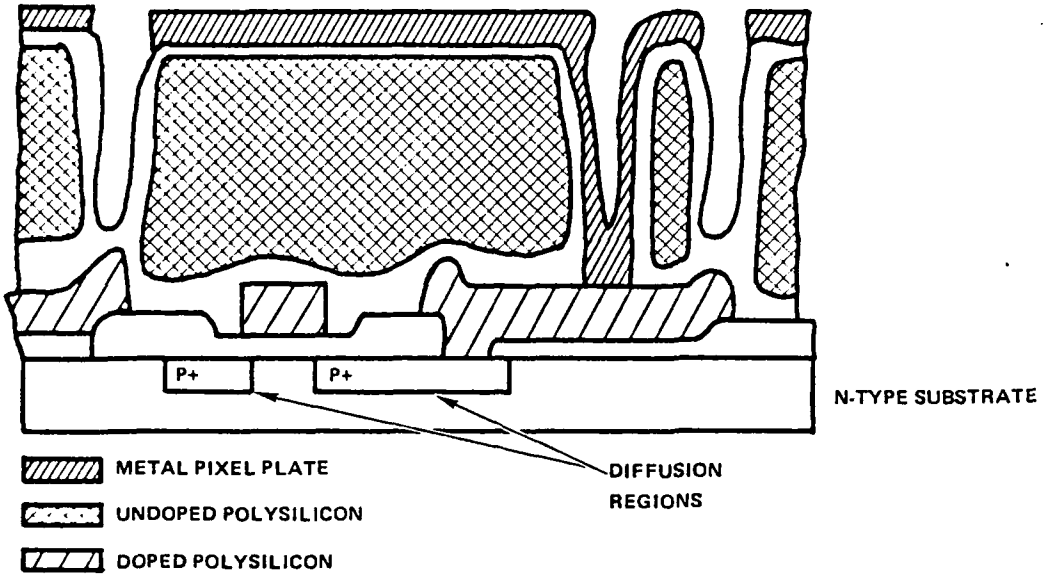
The remainder of this report is organized into four sections. Section 2 summarizes the work performed on the high density (23.1 pixel/mm) display including the problems which led to the redirection of effort. Section 3 covers the display system which was designed and fabricated during that redirected effort. Section 4 discusses the specific tasks undertaken during this program. It includes a discussion of the hardware which was delivered. The final section summarizes the status of current technology and the implications of results obtained for future work in this area.

2.0 The High Density Display With Integrated Drivers

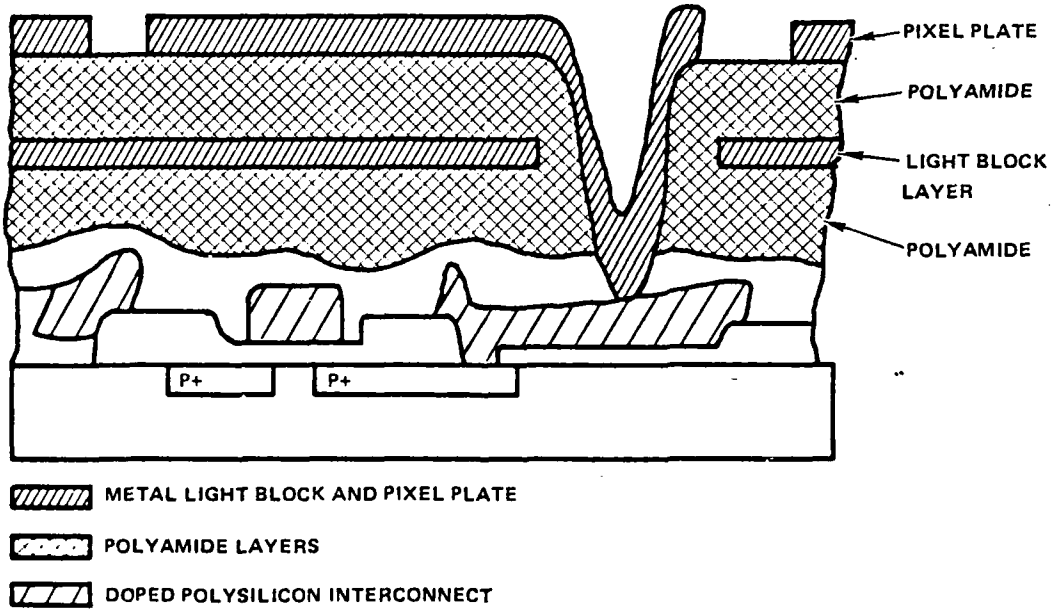
The initial baseline approach for this program was a display with 23.1 pixels/mm which had been designed as an IRD task. This display was based on one developed for a previous Night Vision Labs program. However to minimize interconnection difficulties at that high density it was decided to integrate the display drivers adjacent to the display in the same piece of silicon. The resulting circuit requires only twenty three independent signals to generate a full 240 x 312 pixel television image. Those signals were generated by interface boards which utilized commercial VHF and UHF tuners feeding into a CA3068 integrated IF detector. Horizontal and vertical sync signals were separated from the video by discrete circuitry. A 6.25 MHz clock was generated and fed into an 8 bit shift register thus generating an 8 phase clock for distributing the video signal onto 8 video bus lines. Video from the tuner was processed on the circuit board using an HA 2535 and a LM002. The processed video was then distributed into the 8 video bus lines through a bank of CMOS transmission gates (CD4016A) controlled by the 8 phase clock previously mentioned. The video was buffered with an LM002 in each of the 8 video bus lines, and together with the vertical and horizontal syncs, were used in driving the assembled high density display in its hybrid package configuration. A picture of the electronics unit that was to be used in driving the packaged high density display is shown in Figure 2-1.

2.1 Development of the Integrated Drive Circuits

The drive electronics interface to the high density display consisted of on-chip integrated drive circuits and off-chip circuit boards for processing the standard 525 line TV composite video. The on-chip integrated driver circuits provided an interlaced video



Low Density Pixel Display Cross-Section



Medium Density Pixel Display Cross-Section

Figure 2-8. Comparison Between Low Density and Medium Density Pixel Cross-Section

Experimental results with chrome metal indicated that the metal migrated through the silicon dioxide insulating layers which caused major polysilicon interconnect shorting problems. Similar experiments performed with aluminum metal did not exhibit this problem; however, after subsequent processing of the buried metal wafers through final metal electrode definition, the polysilicon interconnect layer was shorted to the light block layer.

Next, tests were run to develop an intermediate insulator layer between the polysilicon interconnect-buried metal and reflective electrode-buried metal layers, as shown in Figure 2-8. Several intermediate insulator layers were investigated, such as:

Chemical vapor deposited (450°) silox
Polyimide films
Low temperature plasma deposited silicon nitride
Sputter deposited silicon nitride and silicon dioxide

None of these films proved to have adequate integrity in the extremely thin layers (3000A) required by the design. Additionally, the capability of achieving an optically flat display surface was not within the existing technological techniques available in the semiconductor industry. Previous experimental results had confirmed that this "smoothing" operation in which a near optical flatness was achieved over the active-display surface was necessary to attain the desired reflectance and contrast performance parameters. For instance, Figure 2-9 illustrates the reflectance for a smoothed and non-smoothed display surface (about 2:1 reflectance improvement). Further development efforts would be required either to develop the mechanical polishing of an insulator layer or to achieve a "self leveling" insulator film upon which the top chrome reflector electrodes would be patterned.

Therefore, the combined processing difficulties of preventing pinhole shorts and achieving a smoothed surface with the intermediate insulator layers has hindered the final development, fabrication, and assembly of the high density flat panel matrix displays (i.e., the four feasibility modules).

2.3 Testing of the High Density Display

Due to the complexity of the high density display, partitioning of the high density array and integrated driver circuits provided for the independent evaluation of each circuit's principal functions. Throughout the successive stages in the gate and drain driver circuits, test points were provided. Each line in the high density array has a test point provided at either end. In addition, several process and device monitor test circuits were positioned about the display device which provided for continuous process evaluation of device characteristics throughout the process cycle, and for improving the display yield in processing. The various test points incorporated into the processing of the high density display were shown in Figure 2-10.

Minicomputer controlled testing was used to collect the information on display line defects. This information analysis quickly confirmed that

There were several processes which required further development in order to fabricate a high density display which would completely satisfy all performance requirements. These developmental process steps are illustrated as darkened boxes in Figure 2-7. For instance, the integrated driver circuits require a high-value resistance layer to provide a low-current load device for stand-by operation during different intervals in the TV frame period. Development of the processing techniques to repeatably reproduce the high-value resistors within the desired resistance range was actively pursued during the wafer processing phase on this contract.

The high density array also requires a buried metal layer to to eliminate photo-generated leakage current to the pixel transistor from the substrate regions exposed by the gaps in the pixel reflective electrode, between each pixel in the array. The 100 x 100 elemental array supplied on the previously mentioned contract was sensitive to the red end of the visible spectrum since the metal light blocking (LB) layer and the reflective electrode were of polysilicon material. Hughes actively pursued on this contract the development of a non-light sensitive light blocking layer which did not "short out" the display interconnect lines and pixel reflective electrodes. Concurrently with the light block layer development, Hughes pursued the development of intermediate insulating layers which "sandwich" the metal light block layer, thus insulating the light block metal from both underlying interconnect layers and the final metal layer which served as the pixel reflective electrode.

In addition to its electrical properties, at least one of the intermediate insulating layers must provide a "self-leveling" film, or be capable of being mechanically polished. This requirement stems from the reflectance and contrast comparisons performed on low density displays between "smoothed" and "non-smoothed" surfaces. A smoothed (i.e., optically flat surface) display provides a reflectance and contrast ratio approximately double that from a nonsmoothed display. Therefore, the active surface area of the high density array must be smoothed to enable the display performance to meet the requirements set forth in this program. Further discussions on display smoothing are provided in a later section of this report.

2.2.2 Optimization of Processing

In developing the high density display process tests of individual process steps were carried out, especially with the high value resistor, light blocking layer, and insulating dielectric layer. For instance, a major accomplishment was demonstrated by varying the boron implant dose of the undoped polysilicon for the high value resistor layer to bracket the desired resistivity needed by the integrated drivers.

Next, tests were conducted to develop the light blocking layer material (buried metal layer) which was deposited between the polysilicon interconnection layer and the top reflective metal electrode. The two primary candidates for light blocking were chromium and aluminum-silicon metals.

TABLE 2-2

ABBREVIATIONS AND TERMS EMPLOYED

IN DESIGN AND PROCESSING

SILOX	A term from silane (SiH_4) and oxygen (O_2), which designates the reactive deposition that accurs when these gases are combined at high temperature (450°C to 1000°C) to form silicon dioxide (SiO_2) on the silicon substrates.
TEOS	An abbreviation for another source gas, tetraethylorthrosilicate ($Si(OC_2H_5)4$), which when reacted with oxygen at even higher temperatures (600°C to 1000°C) deposits silicon dioxide on the silicon substrates.
CVD	An abbreviation for chemical-vapor-deposition which is a descriptive term for the type of reaction that occurs with silox and TEOS depositions. V-CVD indicates the process is done in a vacuum except for the partial pressures of the source gases.
SI	A standard layout abbreviation for the mask defining the poly-silicon gates, interconnects, or other shapes.
CONT	The mask defining contact holes prior to the SI layer
TO	The mask defining the thin oxide region over the gate, capacitor and the regions where contacts are to be made.
DIF	The mask defining the regions to be doped by diffusion of acceptor or donor atoms from a source gas in a furnace tube.
CS	The mask which defines the areas to be implanted around the transistor to form a barrier or channel stop for carriers which might otherwise cause current leakage.
VIA	The mask forming the deep contact or via through the thick deposited TEOS layer.
CR	The mask defining the chromium matrix on the miniature active matrix device.
LB	The mask defining the holes in the light block or ground plane layer on the miniature active matrix device.
SA	The mask defining the self-aligned source and drain regions which use the gate as the mask for the edge of the implant.

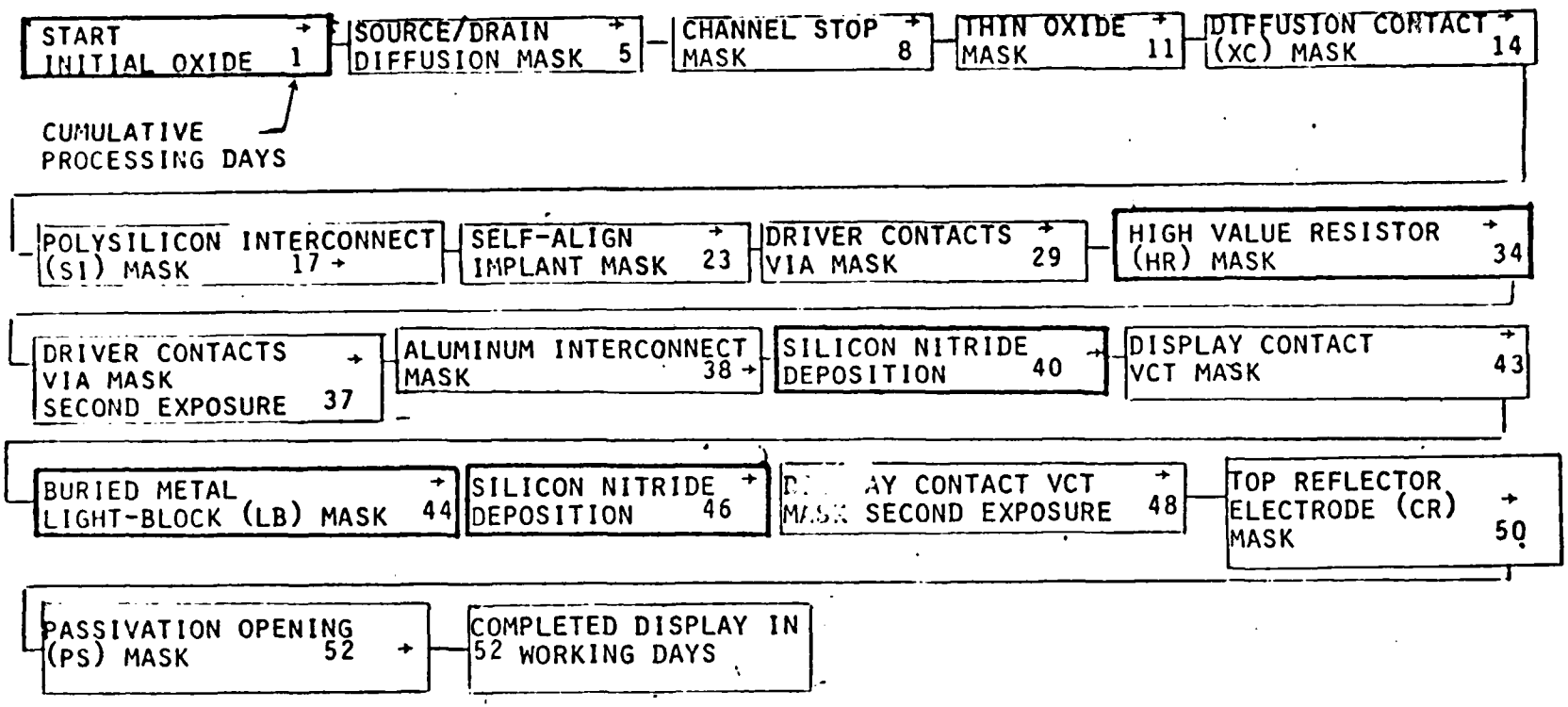


Figure 2- 7. High Density Matrix Display Process Flow Chart

Table 2-1. Characteristics of the High Density Display Design Rules

Process	Layout Rules (Mils)	
	Width	Spacing
p^+ Diffusion	0.3	0.6
n^+ Diffusion	0.3	0.4
Contact Holes	0.2 x 0.2	
P^+ Polysilicon	0.3	0.3
P^+ Implant	0.3	
Cell Geometry	1.7 x 1.7	0.2 Gap
Gate	Self-aligned silicon gate	
Metalization	Double layer: Chrome/Poly	
Light Blocking Layer/ Capacitor	New "Ground Plane" Design; Vertical Capacitor	

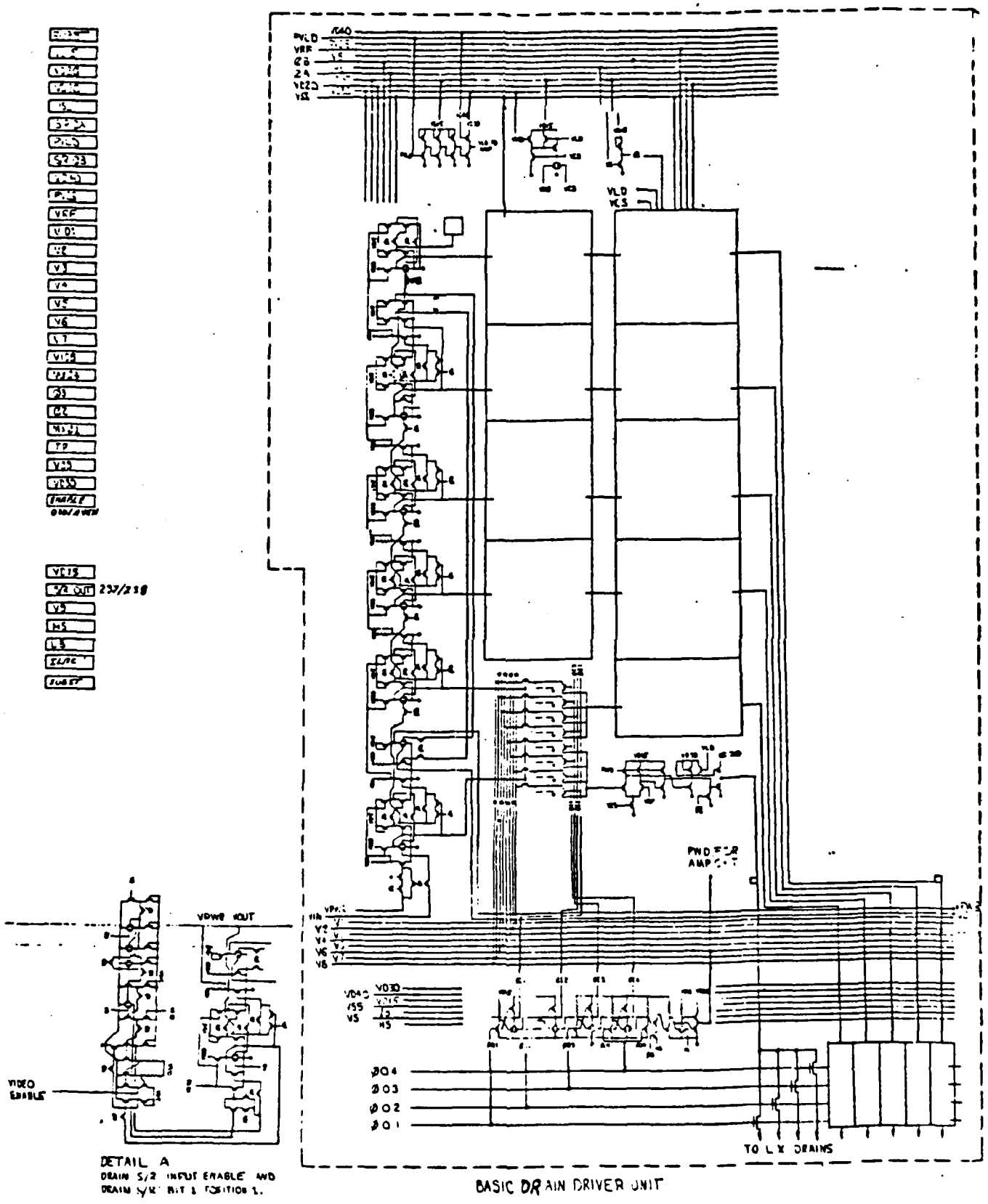


Figure 2-6. Integrated Drain Driver Circuit Schematic

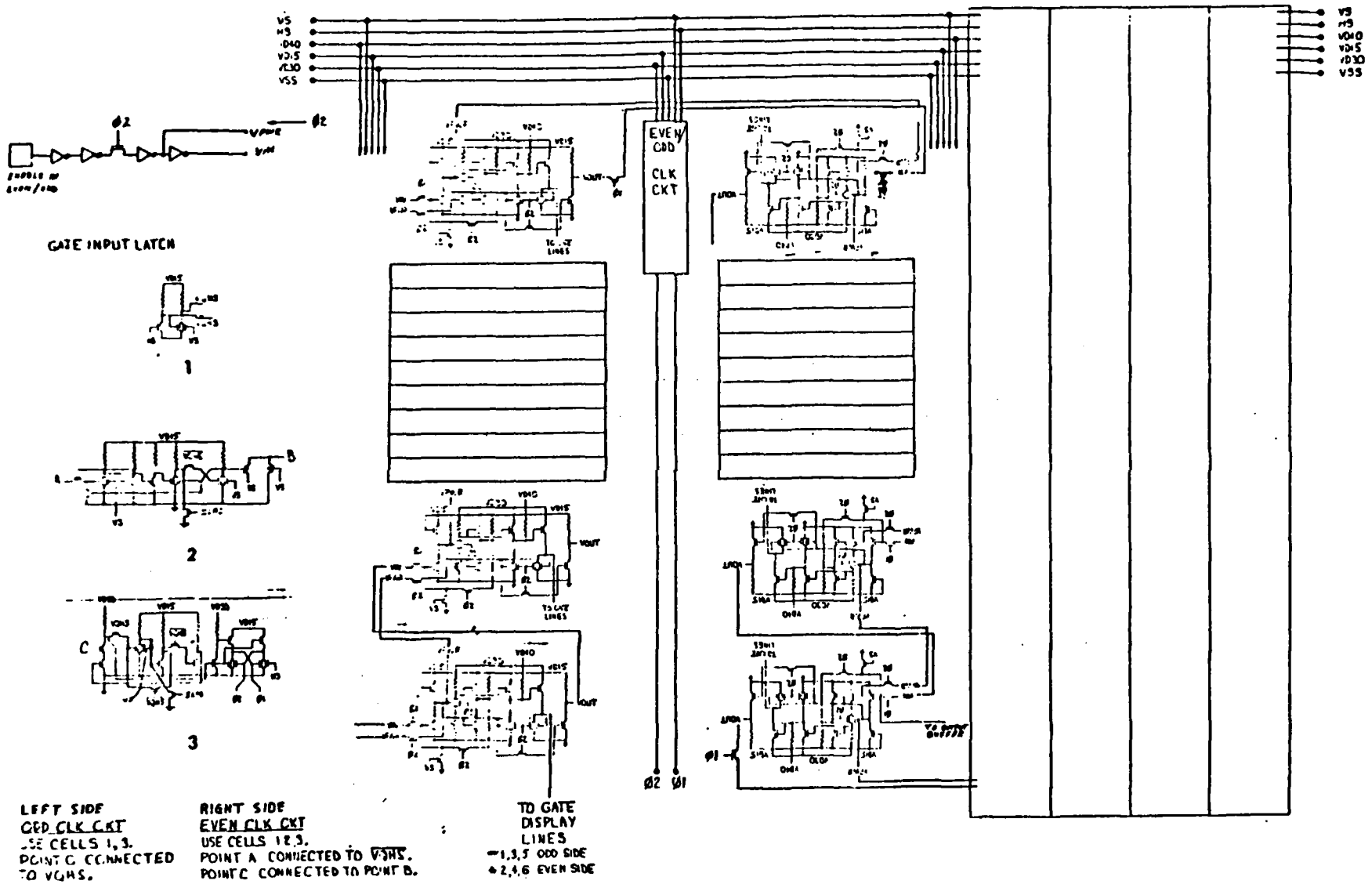


Figure 2-5. Integrated Gate Driver Circuit Schematic

pulse width, is to allow the continued loading of the pixel capacitors with the video sample provided from the drain driver circuits. The gate circuits on both sides of the high density display are powered-down during the video sampling period in a TV frame in order to reduce power dissipation. The schematic for the gate driver circuits, located on either side of the high density pixel array, is shown in Figure 2.5.

2.1.3 Drain Driver Circuit Design

The integrated drain driver circuit consists of several elements, which are described in the following discussion and whose relative position in the high density display is shown in Figure 2-2. There are 78 shift register circuits which control the video sampling from the 8 video buses brought onto the chip from drive electronics interface boards. The 8 video bus lines sample the composite video and amplify it by a factor of 4 at a 12.6 MHz rate. The on-chip shift register string samples the 8 video bus lines at 1.56 MHz. This reduces the power dissipation and required speed of these shift registers to acceptable levels for integration with a high density display. When the shift registers are not used for video sampling, they are powered down, to further reduce their power dissipation. The sampled video signal is stored on a MOS capacitor, and held for a maximum of 53 microseconds, before being read out to the video amplifier circuits. These linear differential amplifiers receive the sampled video signal from four capacitors, in a sequential manner. The video signal is amplified by a factor of five and driven to the corresponding drain line on the high density display. Process compensation circuits, current sources, and alterable bias control circuits are available on chip for the video amplifiers to be compensated across the driver circuit area for uniform video amplification. The schematic for the drain driver circuits, located at the top of the high density pixel array, is shown in Figure 2-6.

2.2 Processing of the High Density Display

2.2.1 High Density Display Processing Requirements

Under a prior contract with the Night Vision Labs, Ft. Belvoir, VA., Hughes produced a line defect-free 100 x 100 element array of 23.1 p/mm resolution. The conservative design rules that were used to achieve this elemental density were also utilized in the new design of the 240 by 312 high pixel density display with integrated drivers. The principle design rules are summarized in Table 2-1. In addition, the same processes and fabrication controls developed for the 100 x 100 elemental array were directly applicable to the high density display and integrated drivers. A description of the high density display process is provided in Figure 2-7.

A description of the semiconductor abbreviations and terms employed in the display and driver designs and in wafer processing is listed in Table 2-2.

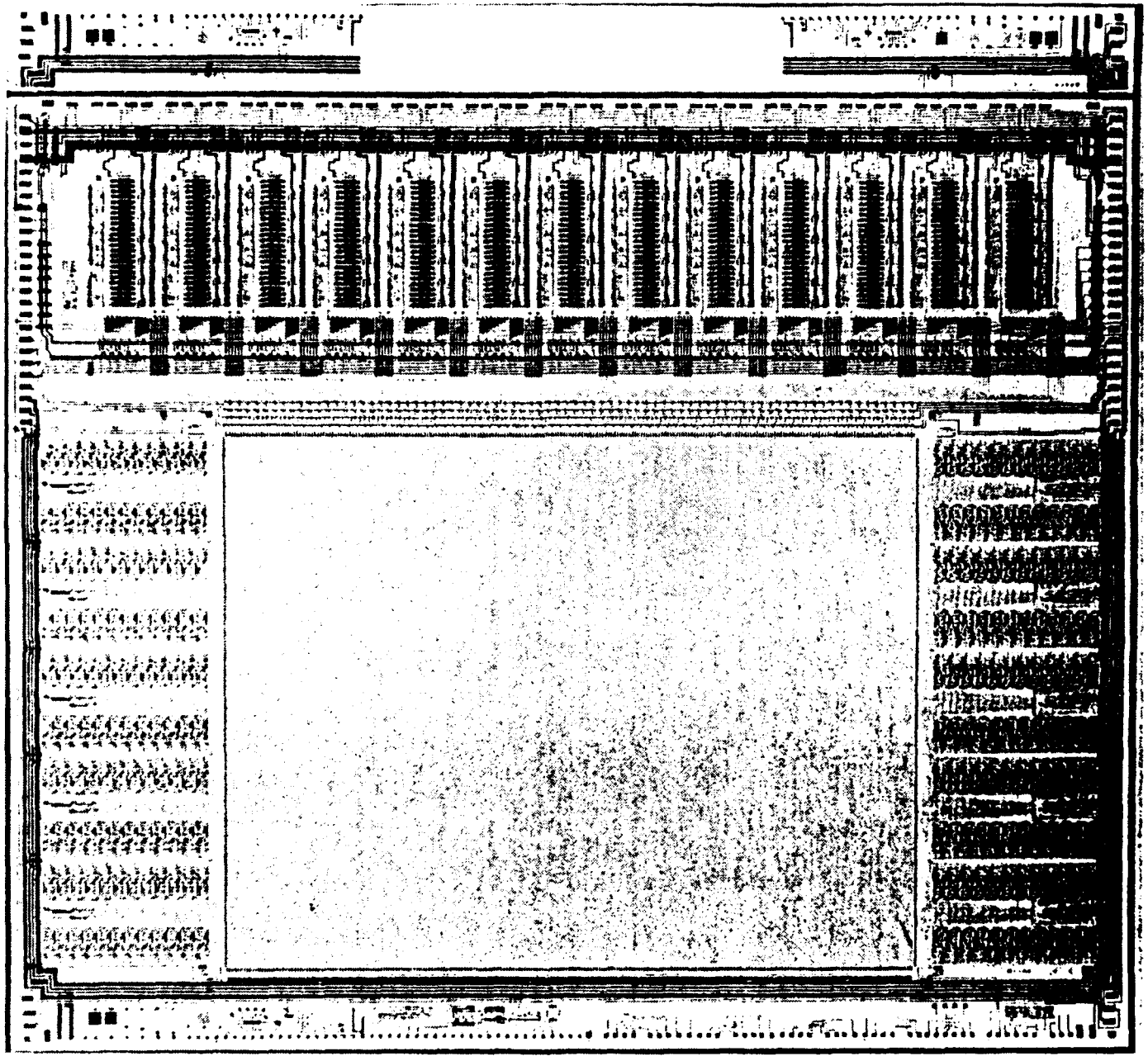


Figure 2-4. High Density Display Layout for H4035 Device

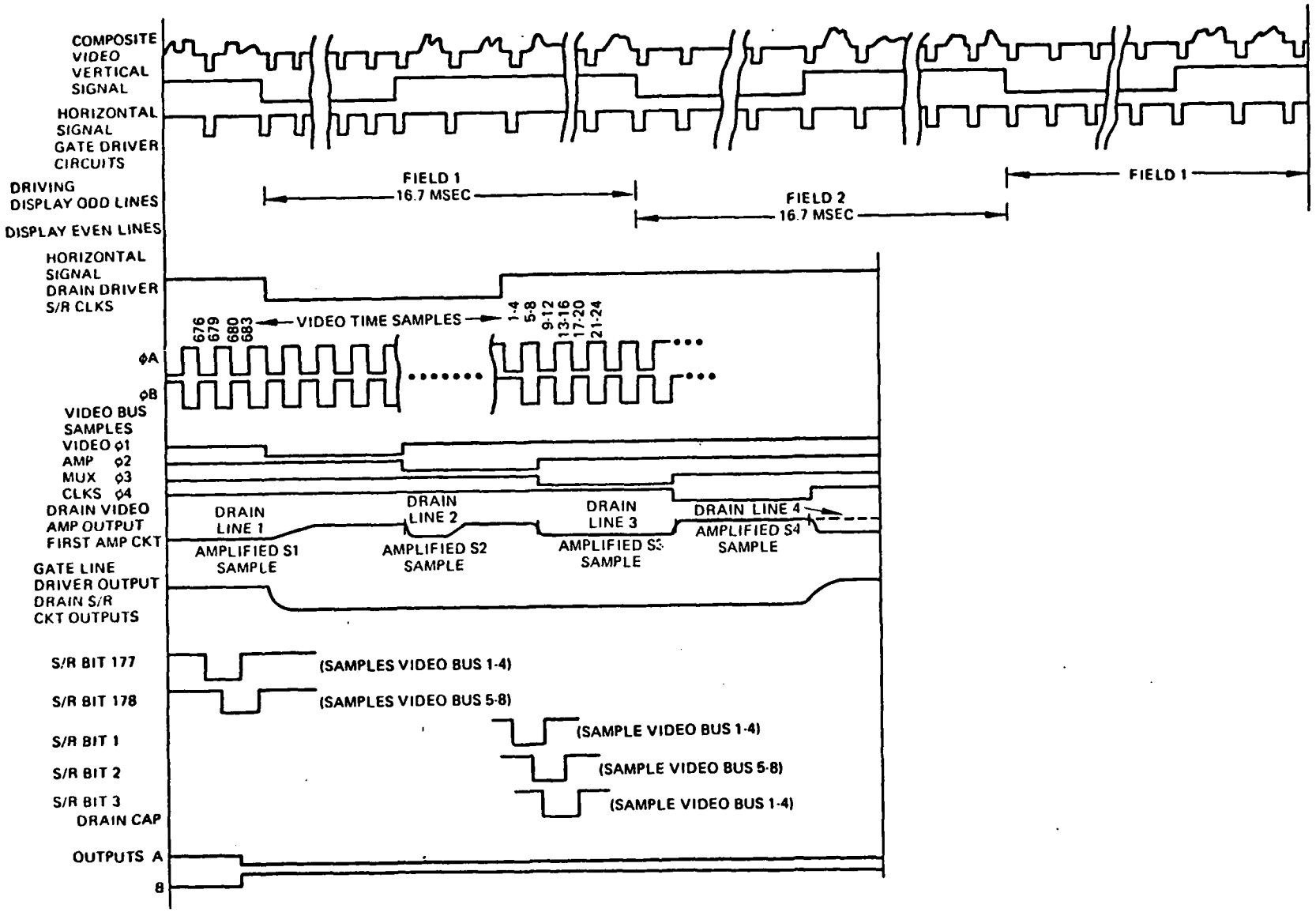


Figure 2.3 High Density Integrated Driver Circuit System Timing Diagram for 525 Line TV Rates

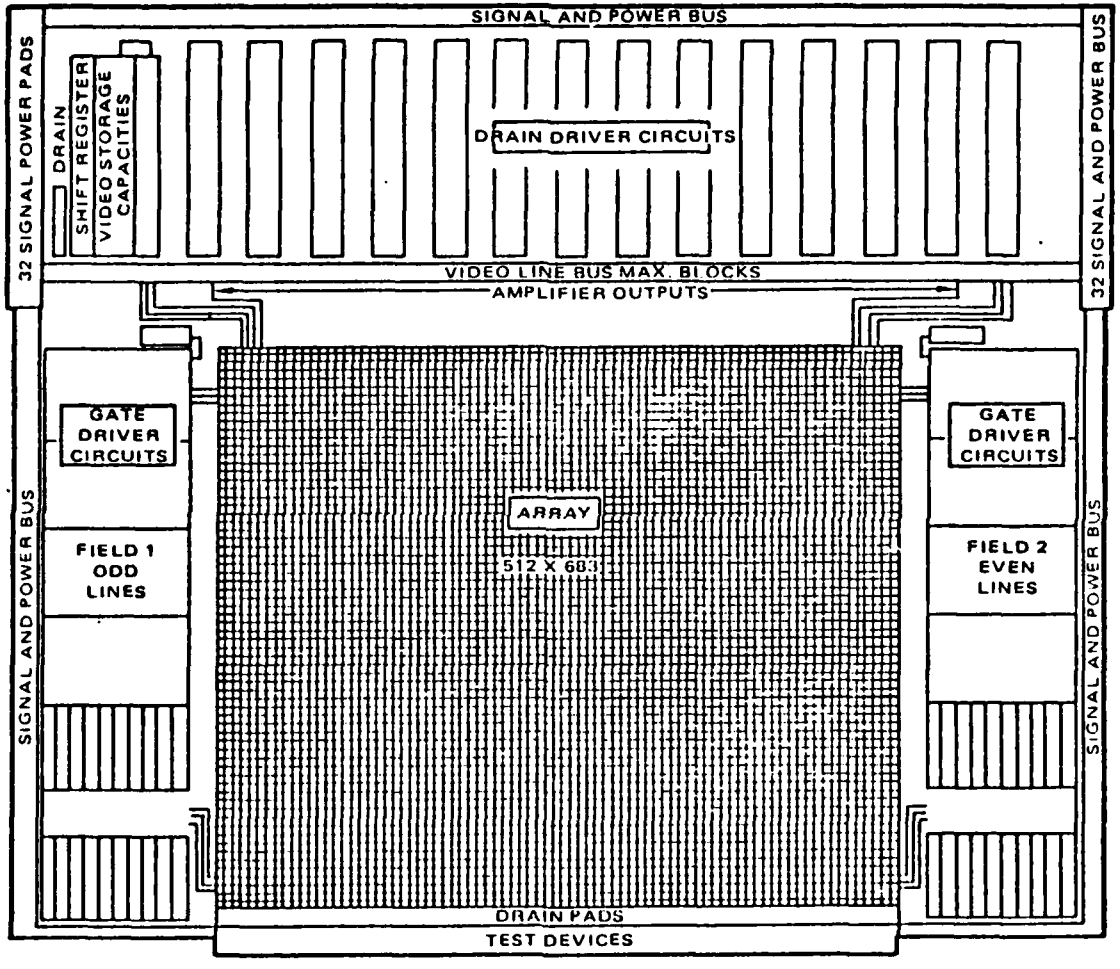


Figure 2.2 High Density Display Chip Layout Schematic

image to the horizontal 240 gate lines and vertical 312 drain lines in the high density array. The resultant high density display layout schematic is shown in Figure 2-2. The integrated driver circuits were implemented with the same 9 photomask p-channel MOS process used to fabricate the high density array, augmented by the addition of four photomask layers for elements of the driver circuits.

Designs of the integrated driver circuits utilized on the high pixel density display have evolved from a series of designs and concepts, some of which have been used on previous driver circuit designs.

2.1.1 Integrated Display and Driver Circuit Design

The integrated driver circuits for the high density display contain essentially two different design types. The gate driver circuit controls the sequential activation of the horizontal gate lines. The interconnections between the gate driver circuits and the display gate lines provide the display with interlaced video signals at the frame rate of 30fps. The drain driver circuits select the video signal samples which are then placed on the display. These circuits provide the high density display with a line of video information at the same time the gate driver circuits activate the corresponding horizontal gate line on the display. A timing diagram is shown in Figure 2-3 for the integrated gate and drain driver circuits that were used on the high density display. Each of these designs will be discussed in greater detail below.

An evaluation of the high density cell concepts and integrated driver configuration resulted in the design and layout of the high density display circuit shown in Figure 2-4. Several of the significant layout characteristics are described as follows: The gate driver circuits were positioned on both sides of the display whereas the drain driver circuits were positioned at the top of the display. Process monitor devices and critical driver circuit elements (i.e. video amplifier circuit) were positioned in an area approximately .15 cm wide around the display's active image-area. The high density display design, layout, and photomasks were previously developed on an Internal Research and Development (IR&D) task which undertook the implementation of a MOS matrix display with a high pixel density configuration. The resulting high density display layout was positioned as two arrays on a 3 inch silicon wafer by utilizing a thirteen photomask sequence.

2.1.2 Gate Driver Circuit Design

The integrated gate driver circuit consists of two strings of 2 phase registers located on either side of the high density display. The line drivers on the left side of the display are connected to the odd numbered horizontal gate lines. Likewise, the gate drivers on the right side are connected to the even numbered horizontal gate lines. Each gate driver shift register string contains its own on-chip, 2 phase, clock generator which is activated by horizontal sync pulses in the video field that is being displayed. The increased time duration, shown in Figure 2-3, for the gate line driver output, beyond the horizontal sync

Figure 2.1 Electronics Interface Boards for Driving the High Density Display

NOTES: Board A is the video sync stripper circuits
Board B is the video multiplexer circuits
Board C is the programable clock circuits
Board D is the video and clock driver circuits

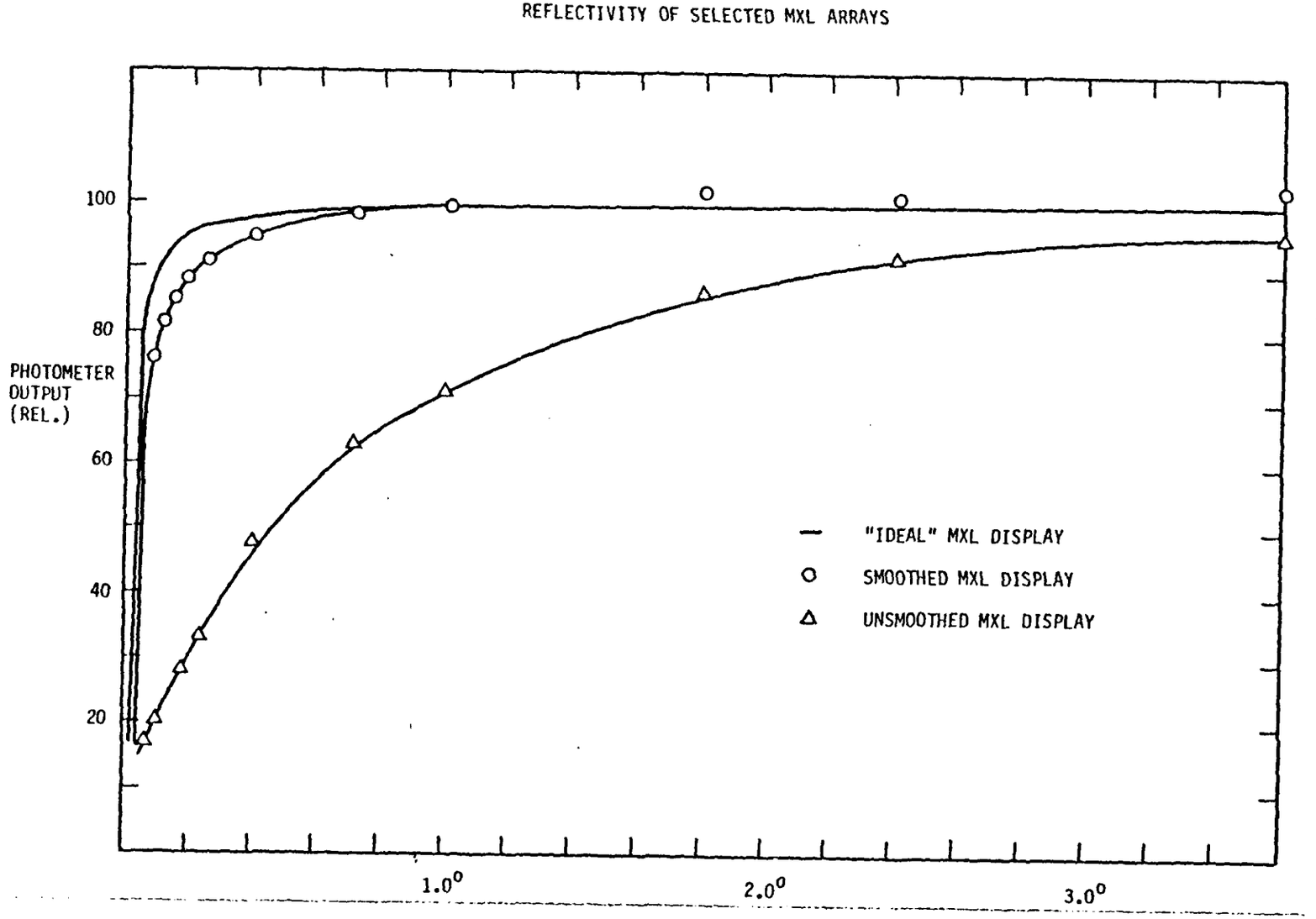
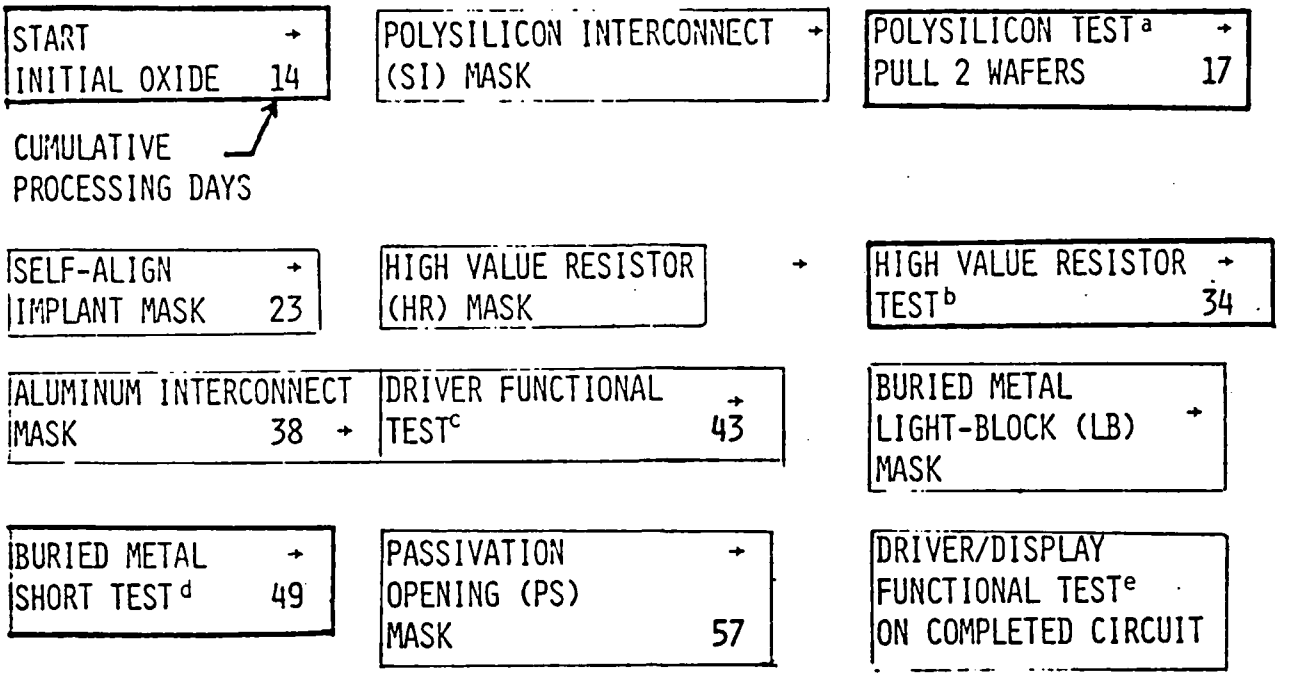


Figure 2-9. Comparison Between Reflectance on a Smoothed Versus Nonsmoothed Low Density Matrix Display



TEST POINTS	PURPOSE
a POLYSILICON TEST	DEVICE THRESHOLD DIFFUSION & POLYSILICON INTERCONNECT RESISTANCE DIFFUSION REVERSE JUNCTION BREAKDOWN
b HIGH VALUE RESISTOR TEST	VALUE OF PATTERNED RESISTOR MATERIAL
c DRIVER FUNCTIONAL TEST	GATE DRIVER SIGNALS TO DISPLAY DRAIN DRIVER SIGNALS TO DISPLAY
d BURIED METAL SHORT TEST	EVALUATE LIGHT BLOCK METAL STEP COVERAGE EVALUATE INTEGRITY OF INSULATOR
e DRIVER/DISPLAY FUNCTIONAL TEST	EVALUATE LIQUID CRYSTAL DISPLAY ASSEMBLED AS DEMOUNTABLE ON WAFER TEST STATION. EVALUATE GATE & DRAIN DRIVER SIGNALS TO DISPLAY

Figure 2-10 High Density Display Testing Flow Diagram

the display photomask set was free of any defects that would adversely affect the display or driver circuit operation. The analysis of the driver circuits and process monitor circuits was performed on the Electroglas test station shown in Figure 2-11.

2.3.1 Integrated Driver Circuit Tests

Test points were provided in the drain and gate driver circuits, at every twelveth shift register bit, for sampling the correct propagation of the activation pulse. In the drain driver circuits, test points were placed on every video amplifier output to monitor the uniformity of the amplified video signals from all 78 amplifiers across the top of the display circuit.

Test points were also placed in each on-chip clock circuit used by the gate driver circuit.

2.3.2 High Density Display Tests

Test points were provided on each end of every line in the high density array. The electrical tests detected the number of shorted or open lines in the pixel array. Independent of the driver circuit performance, a test circuit of the display pixel elements, a 4 x 4 matrix, was used to evaluate the high density display characteristics. This test matrix allowed for the evaluation of the pixel cells without the gate and drain lines of the large display affecting its performance.

2.3.3 Process Monitor Tests

Test circuits were provided to monitor the process parameters of the high density display as it was being processed. For instance, these circuits provided for the monitoring of device thresholds, interconnect line resistance and continuity, contact resistance between interconnect lines, reverse biased breakdown voltage, and leakage currents of implanted and diffused regions in the silicon substrate. In addition, these circuits allowed for the evaluation of the insulating qualities of the various silicon dioxide and silicon nitride layers used throughout the process cycles.

2.3.4 Wafer Production And Evaluation

For the high density display, there were twelve wafer lots (each consisting of 20 three inch wafers) processed through the various steps of the semiconductor processing flow charts shown in Figure 2-7. Typically, two wafer lots per month were started into processing. The average throughput of a wafer lot to the aluminum functional test point was sixteen weeks.

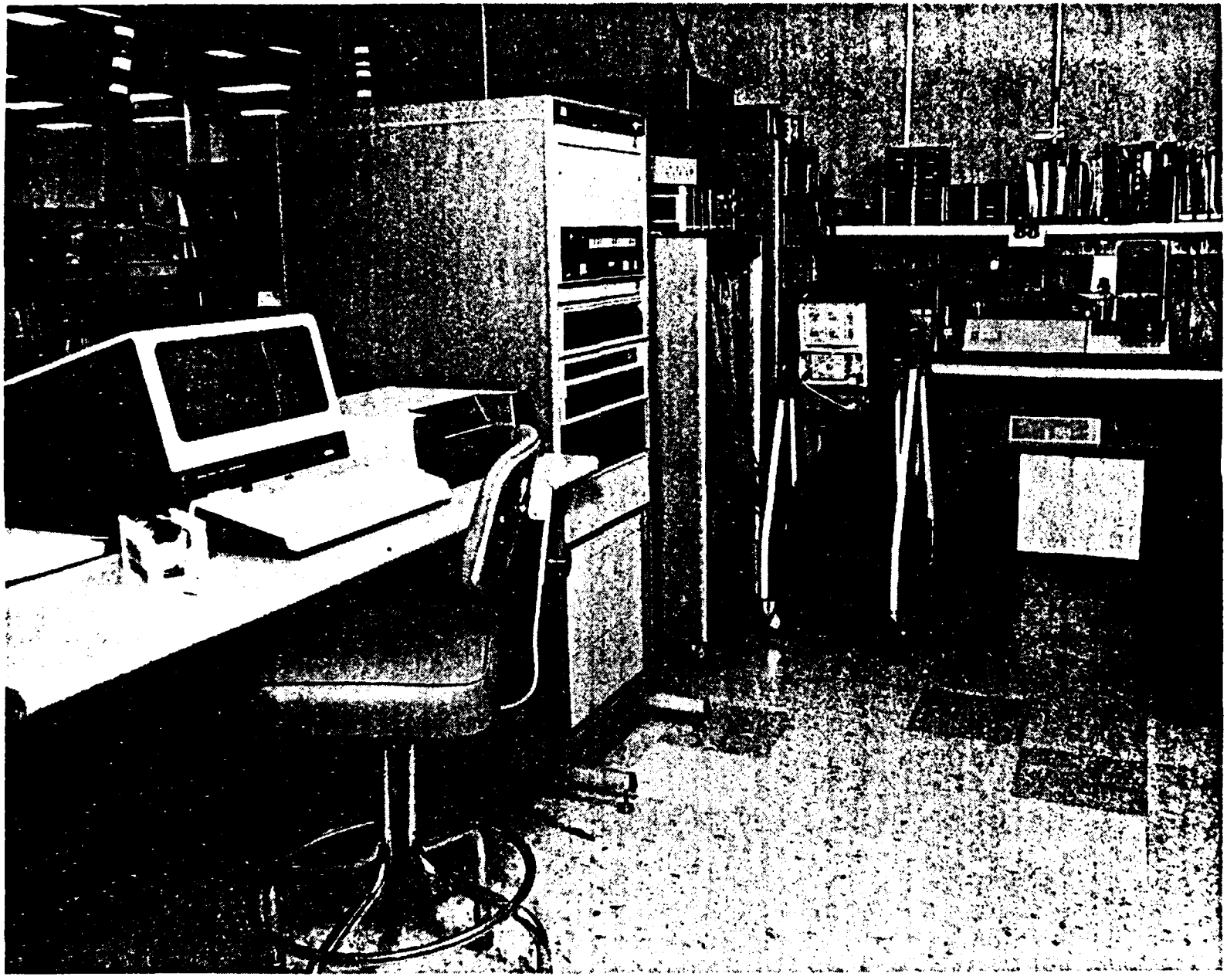


Figure 2-11. Automated Computer Test Station With Electroglas Prober

Processing parameters and transistor operational characteristics were obtained from most every wafer processed. The evaluation of wafer lots at intermediate test points (illustrated in Figure 2-10) provided the necessary feedback in optimizing the performance of the high density displays for the feasibility modules. For instance, the evaluation of test wafer lots and display characterization provided the necessary information to direct the process modifications for achieving the specified resistance values in the high value resistors. The silicon nitride and sputtered silicon dioxide test lots provided the necessary feedback for evaluating these materials as intermediate insulator layers.

The high density display characterization demonstrated functional gate and drain driver circuits. The characterization of the gate driver circuit indicated the design was satisfactory and provided the necessary signals and timing for the video displays, as shown in Figure 2-3. The wafer characterization did suggest that the photomask set was free of defects which might otherwise inhibit the fabrication of a totally functional display. The gate driver outputs supplied 30 volt pulses to the display gate lines, and dissipated 0.3 watts. The characterization of the drain driver circuits indicated that there was a design error in a part of the shift register section. However, the majority of the drain driver circuit design was characterized by micro-probing and generating shift register signals to compensate for the design error. All of the other major circuit elements in the drain driver design functioned as anticipated. For instance, the video on-chip amplifiers provided a uniform 0-20 volt output waveform with an acceptable variation of +/-0.25 volts. The characteristics of the video amplifier, video storage elements, and on-chip multiplexing circuits were demonstrated satisfactorily, as to the expected waveforms shown in Figure 2-3.

A design correction in the drain shift register section was made and implemented on several display wafer lots. However, the wafer lots and further evaluation efforts have been placed on hold, after the redirection of the program's efforts by the Tri Service committee.

2.4 High Density Display Assembly and Packaging

After the wafer processing and final electrical tests were completed, finished high density displays were sawed to the proper dimensions and then mounted to thermally conductive circuit plates with a suitable epoxy. A diagram of the assembly and packaging operations is provided in Figure 2-12. The previous interconnection techniques for interfacing the driver circuits to large area liquid crystal displays were not viable for high density displays because of the extremely large number of connections and leads that would be required. In order that the final package size be minimized and meet the program volume requirements, the video and gate driver circuits were integrated with the array. Thus, the electronics interface encompassed only the clock pulses, video signal buses, and power supplies, which were provided to

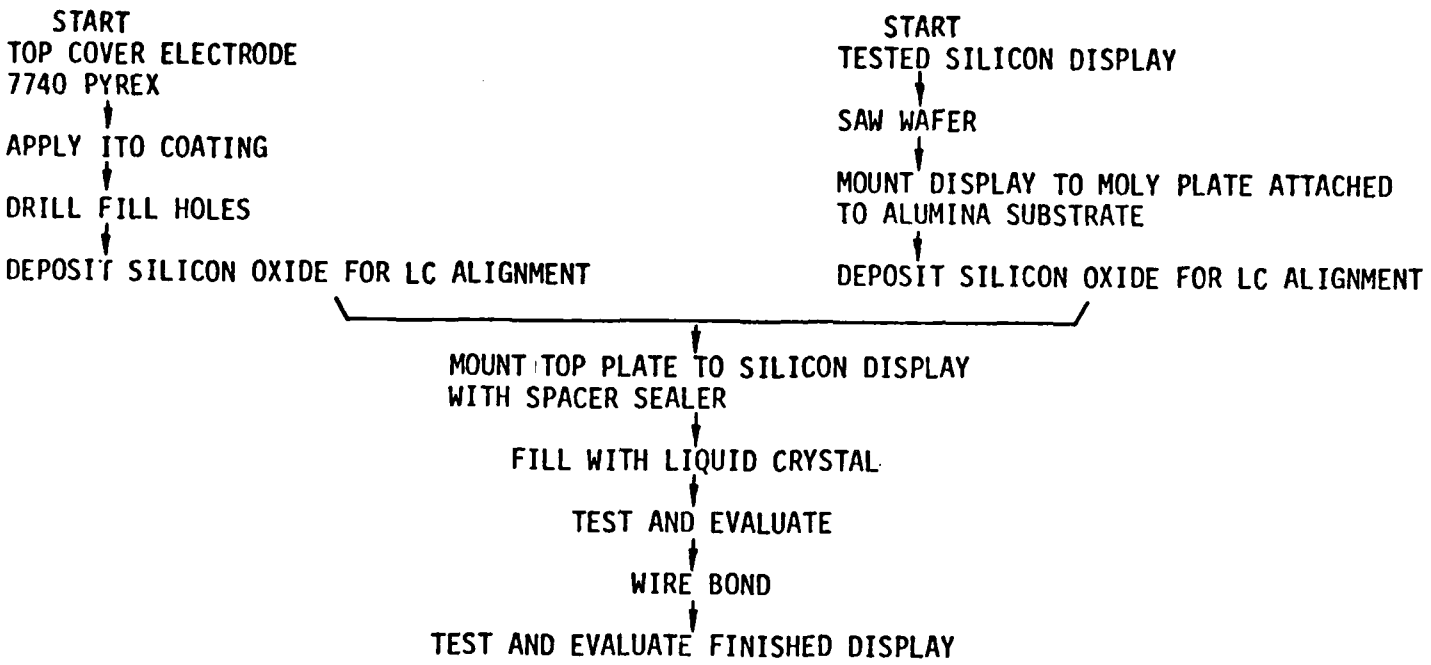


Figure 2-12. High Density Display Packaging Flow Chart

the display's circuit plate connectors. This packaging configuration required just 23 signal lines between the electronics interface and the display package. The package cross-section is illustrated in Figure 2-13 and shown with the electronics interface box, in Figure 2-14.

Several of the high density display's packaging concepts required additional development, in order that the assembly techniques were repeatable and provided high yields. For instance, we had to establish the appropriate sequence for assembling the thermally conductive package, evaluate epoxies that were compatible with the thermal expansion between the display and circuit plate, and devise the interconnect mechanism for interfacing the electronics board to the display's circuit plate connectors.

In addition, the mylar spacer placed between the top glass plate and the silicon display was chosen as 6 microns thick instead of the previous standard 12 microns in order to minimize the liquid crystal speed of response. The definition of the display assembly technique incorporated the results of a thermal analysis study. The significant conclusions of this thermal analysis are shown in Appendix B.

Two high density displays were assembled and wire bonded on the alumina circuit plate. However, inter-layer shorting on these displays prevented them from functionally operating. The application of a dc bias from top plate to display substrate did activate the liquid crystal uniformly across the active area in each of the displays. The development of cell assembly techniques has progressed as far as possible on non-functional displays. Further work on cell assembly development was awaiting the development of operational high density displays which did not contain inter-layer shorting problems.

2.5 Redirection of the Program

At a project review meeting held July 31, 1979 it was decided that several technological problems had developed with the high density display for which no easy solutions were readily apparent. These problem areas included the integrity of the thin (3000A) insulating layers used to form the vertical capacitor structure as well as the difficulty in obtaining improved image contrast and brightness through smoothing of the display. At a series of meetings in the following week a redirection of remaining efforts on the program was decided on. This involved the design and fabrication of a new display which had medium pixel density (12.25 pixel/mm). This density was chosen as being the highest one compatible with the device structure currently in use for low density (3.91 pixel/mm) displays. Details of that proposed redirection are included in Appendix C.

The remainder of this report will concern, for the most part, results obtained on this redirected effort.

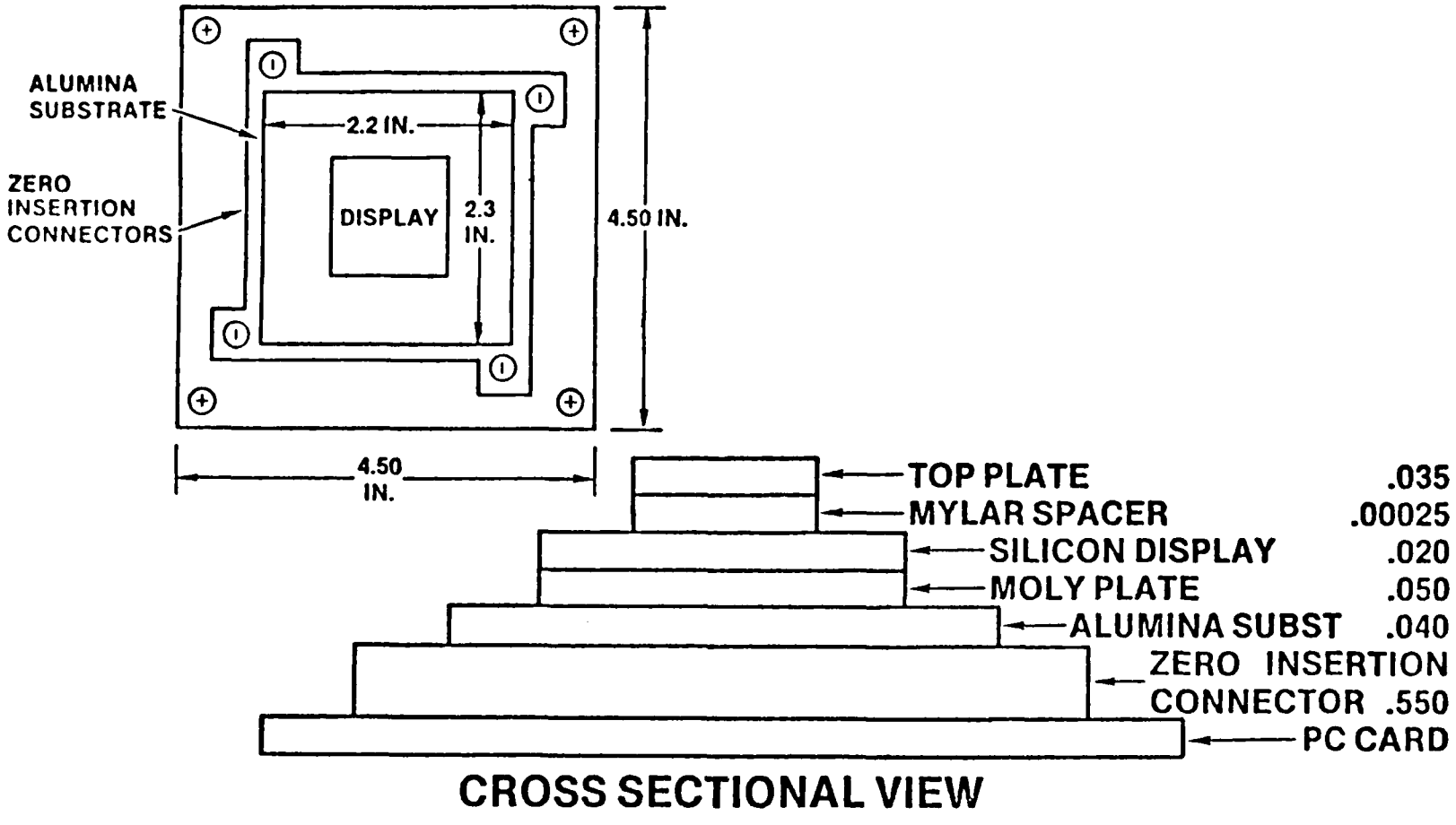


Figure 2-13. High Density Display Package Cross-Section

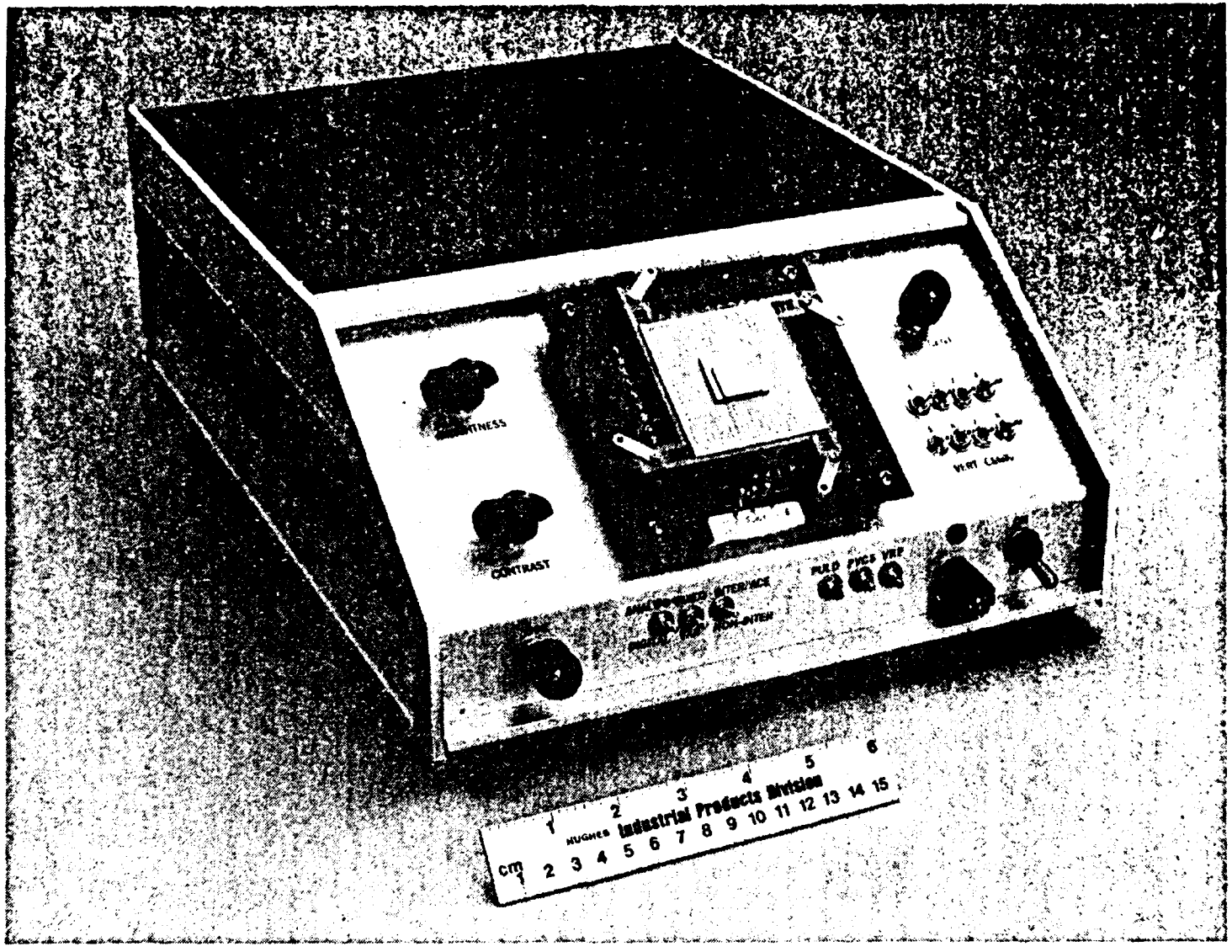


Figure 2-14. Electronics Box Module for Driving the High Density Display

3.0 THE MEDIUM DENSITY LIQUID CRYSTAL DISPLAY

The medium density display system was conceived as a display only (with no integrated drivers) which would be interfaced in a straightforward manner to existing electronics designed for the low density (3.94 pixel/mm) display. This restricted the activated display area to only 175 x 175 pixels, since that was the total number of pixels drivable from those electronics. Those electronics presuppose driving a display on a pyrex circuit plate with leads connected at a 3.94/mm density. Since the patterns on the display device are much denser than that, a study was undertaken to test interconnection capabilities at higher densities, using wirebonding. Wirebonding was chosen because of its straightforward nature and also because of experience obtained on other displays at lower density.

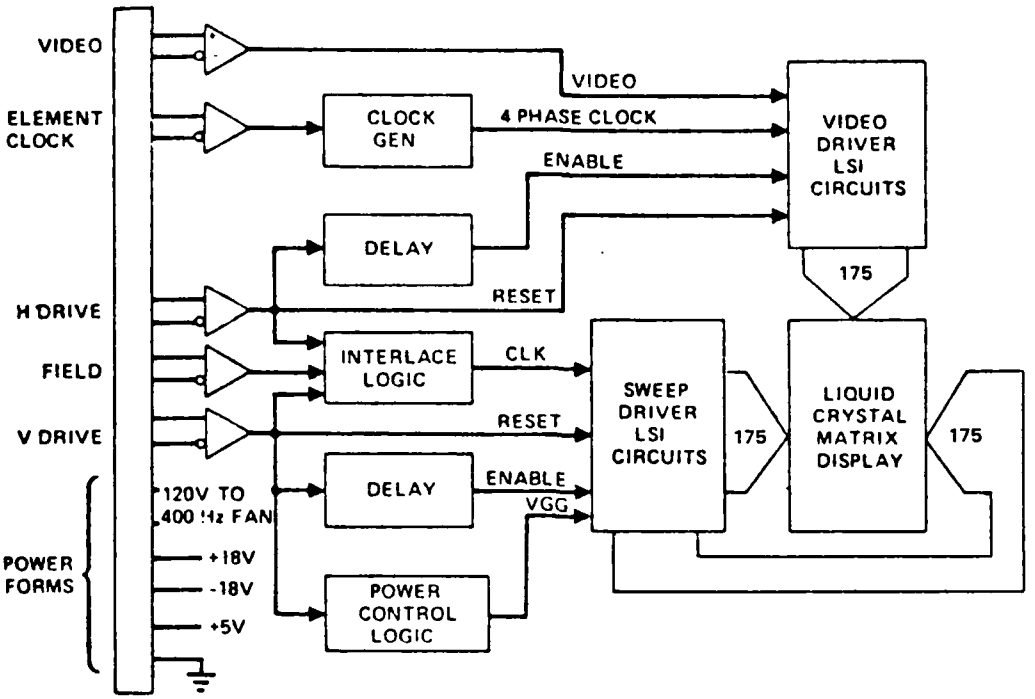
As illustrated in Figure 3-1, the interface to the medium density display consist of four power forms plus the following signals: analog video, element clock, horizontal drive, vertical drive, and field sync. This interface was chosen of necessity; power supplies and sync and clock generation circuitry would not fit into the feasibility display module without using costly, high risk, hybrid circuit packaging for the display drivers and interface circuits.

A new circuit plate was designed to allow driving the medium density display lines with the existing set of interconnect cables and driver boards. However, the cables would only allow the center display sector of 175 by 175 pixels to be activated. As described in the following section, the electronics demonstration boxes utilize copies of the IHUD driverboards, driver circuits, and kapton interconnect cables. The package cross-section and electronics interface box is illustrated in Figure 3-2, for the medium density display.

3.1 Evaluation of Bonding Capability

The purpose of this task was to establish the upper limit of bonding density between two adjacent MOS circuits. The bonds were evaluated on the basis of their ability to meet MIL-STD-883 requirements.

The attached Figure 3-3 summarizes the results from the bonding density study performed by the presently available personnel and equipment. Samples of the bond study test vehicles are shown in Figure 3-4. Evaluation of the individual bonds from one MOS chip to another MOS chip included both electrical continuity and visual inspection of quality control using MIL-STD-883 for setting the acceptance criteria. The second test vehicle method utilized .001 inch aluminum bonds from the



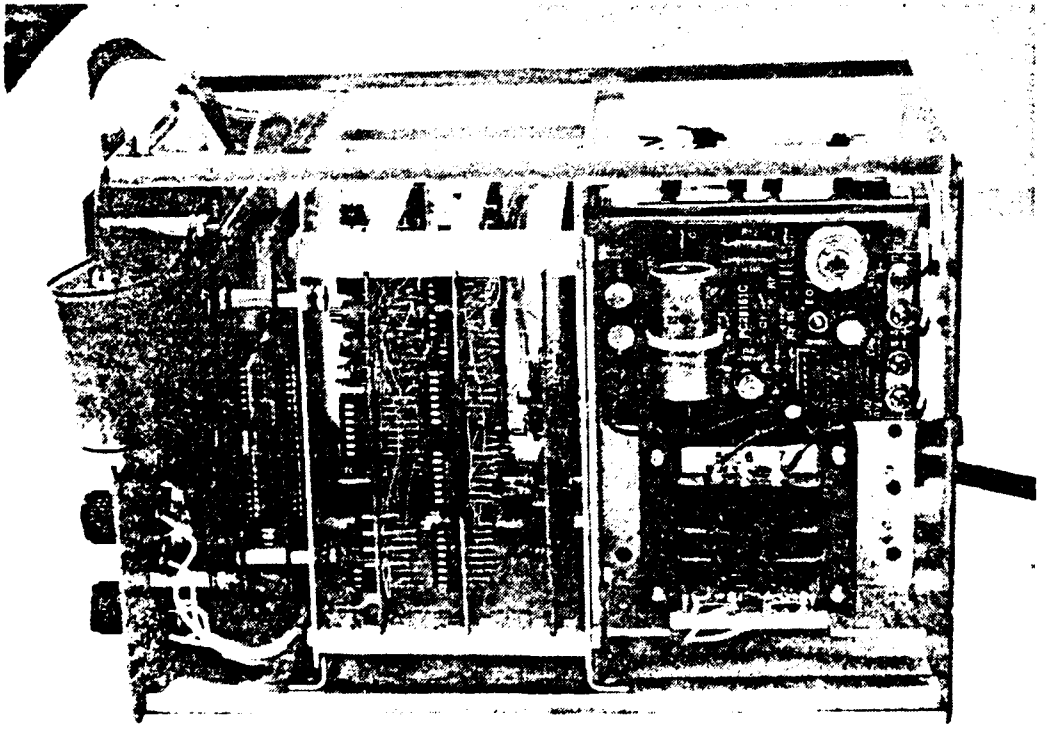
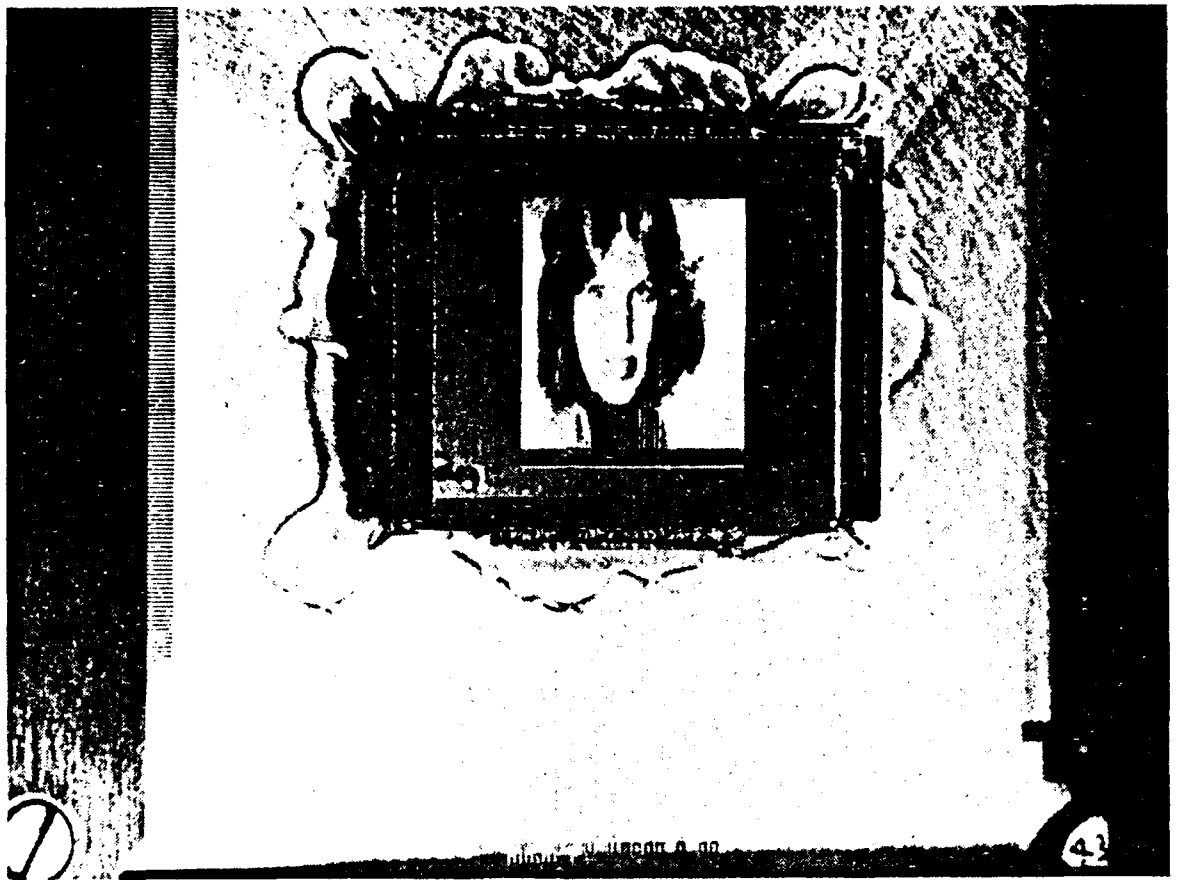


Figure 3-1 Electronics Interface Boards for Driving the Medium Density Display



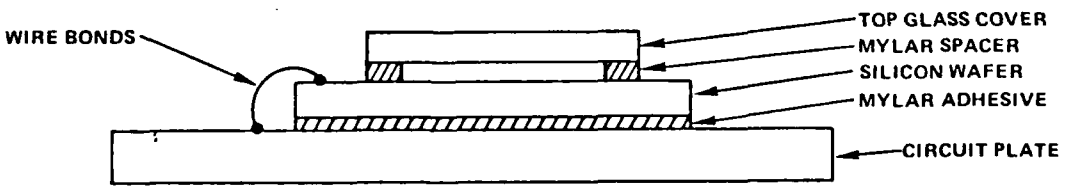


Figure 3-2. Medium Density Display Package Cross-Section

Medium Density Bond Study Results
Using Al Wire, .001 Inch Diameter, Ultrasonic Method

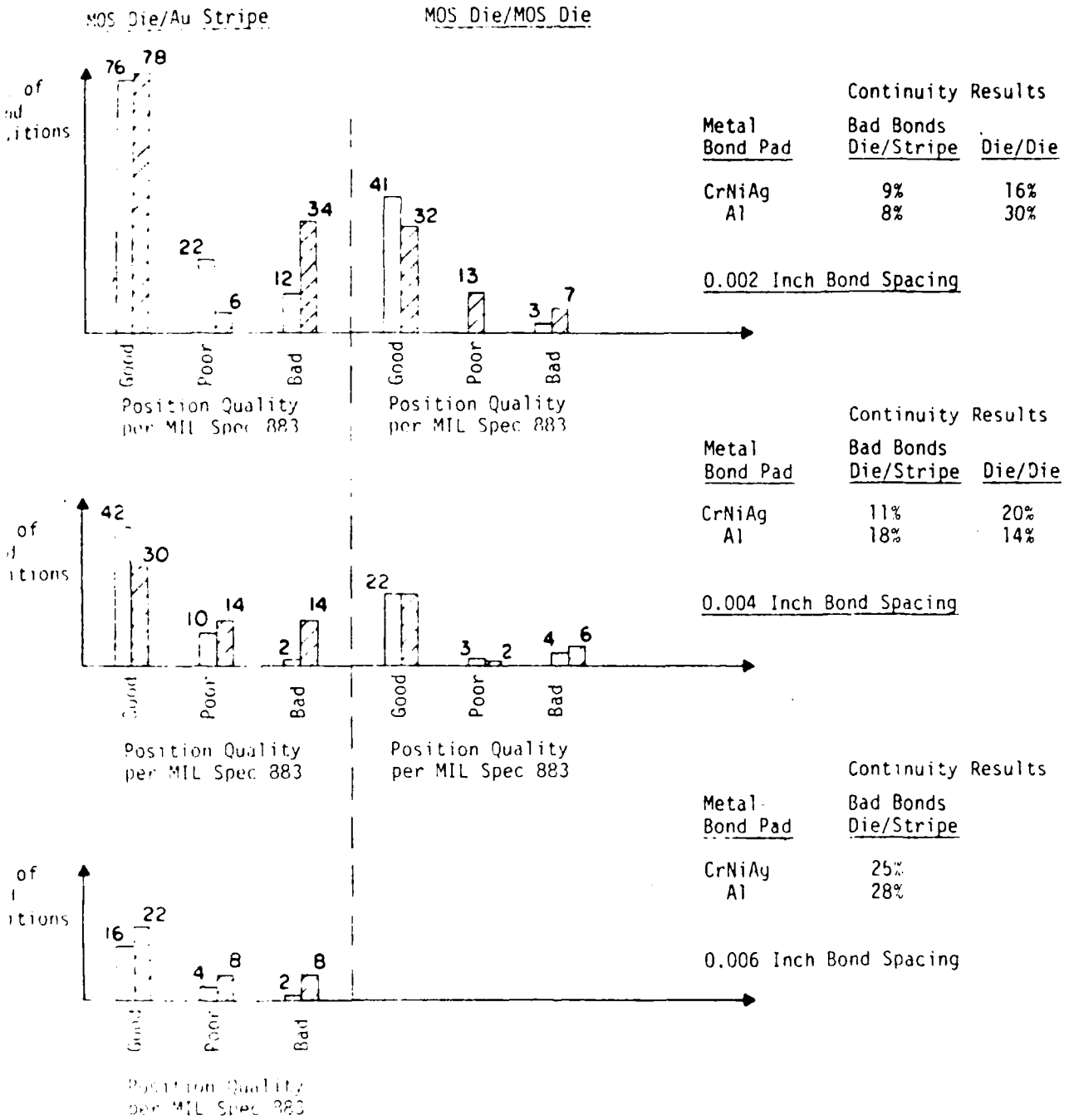
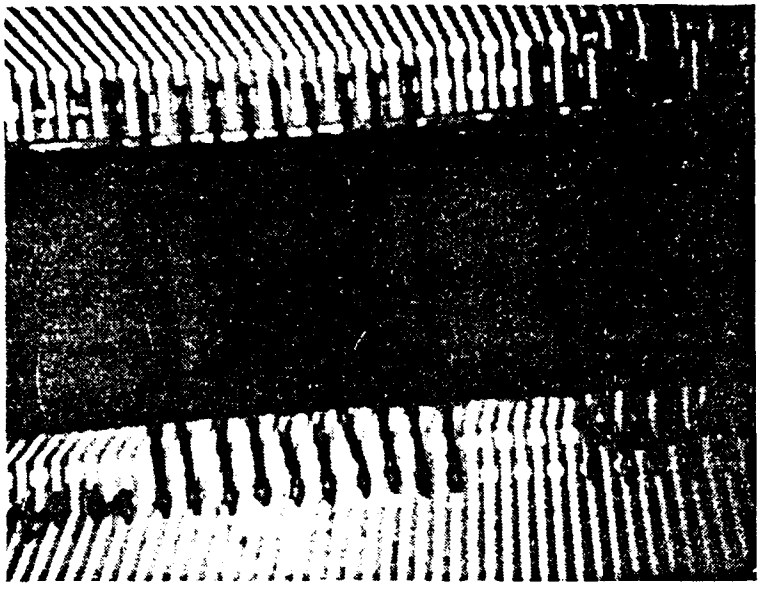
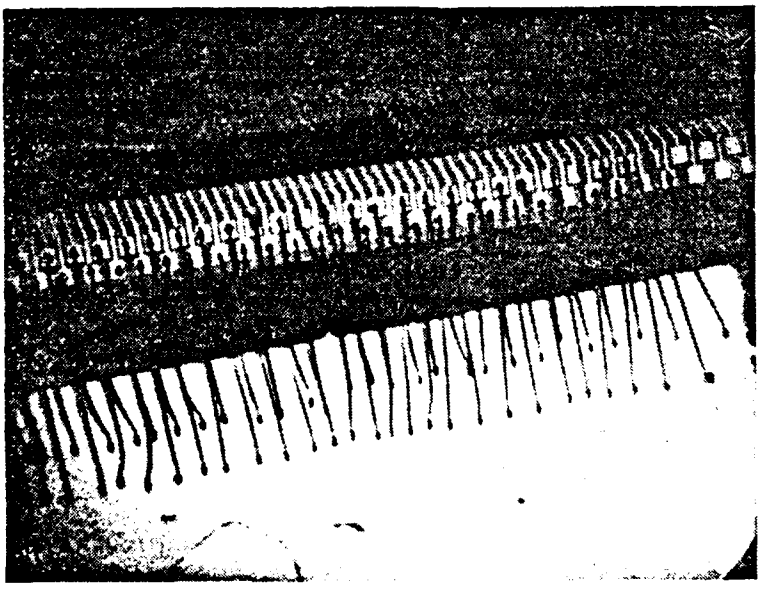


Figure 3.3 Summary of Bonding Study Results

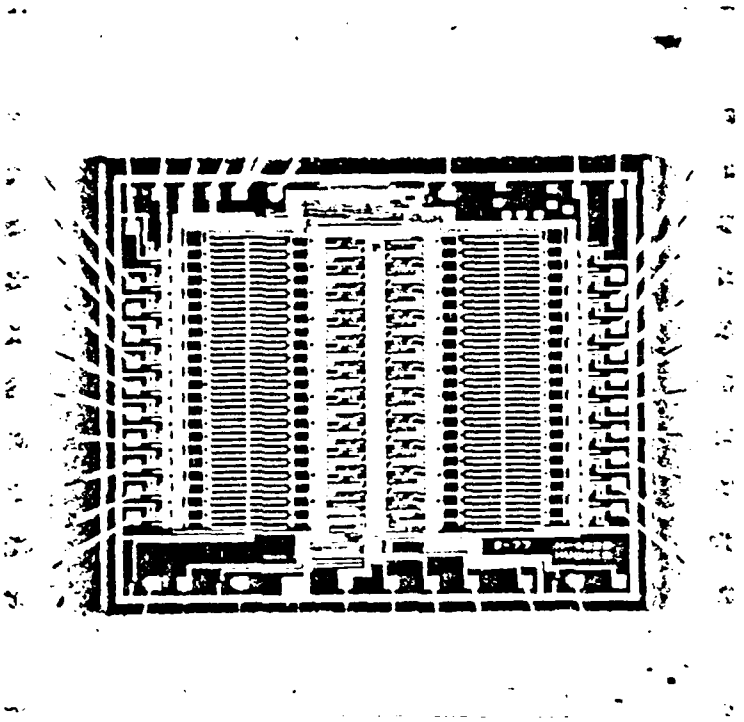


.004 INCH BOND CENTERS
MOS CHIP TO MOS CHIP

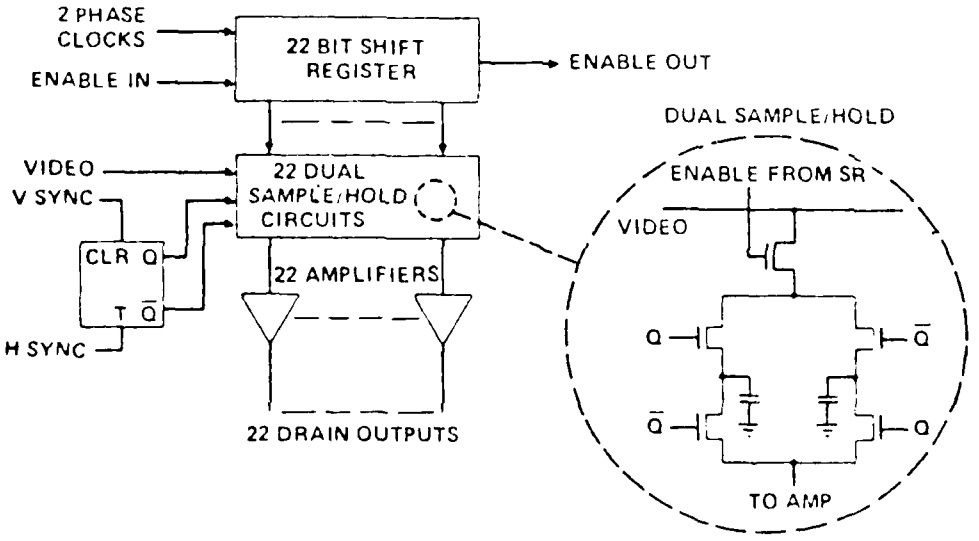


.002 INCH BOND CENTERS
GLASS PLATE TO MOS CHIP

Figure 3-4. Bonding Study Samples



Drain driver circuit layout



Drain driver circuit block diagram.

Figure 3-13. H4022 Custom Integrated LC/MOS Driver

On successive lines, a double clock pulse is applied. Since the spacing between these pulses is short compared to the response time of the driver buffer amplifiers, alternate outputs are skipped over. Similar timing is used during field two, except that a double clock is also applied on the first line. When all 35 outputs from a given circuit have been enabled, the Enable-Out signal propagates to the Enable-In input of the next circuit.

Five sweep driver LSI circuits are mounted on a single pc-board having provisions for attaching two flat cables to drive both the left and right sides of the display. Since each circuit can drive thirty-five display rows, one pc-board can drive 175 rows.

3.4.4 Discrete Drain Driver Design

The discrete drain driver circuit, shown in Figure 3-13, consists of three functional areas, the shift register, the data storage, and the line drivers. The shift register serves to propagate an enable signal such that the video samples for each column of the display are taken at sequential time intervals. The sampled data is stored in two banks of data bins; one accumulates the new line while the other one outputs the samples accumulated for the prior line. Switching between the two banks is controlled by a single flip-flop which is toggled by the horizontal sync signal. The line drivers provide impedance matching; their high input impedance prevents the voltage on the data storage capacitor from changing significantly while their low output impedance assures that the column electrode busses (n lines) respond rapidly to new signals.

A key design feature of these chips is the interlaced sampling sequence. The chips are grouped together in sets of four, and they are driven from a four phase clock such that the first chip takes the first sample, the second chip the second sample, etc., until the fifth sample which is again taken by the first chip. A timing diagram for a given chip is shown in Figure 3-14 and the output interlacing required for placing all the outputs in sequential order is shown in Figure 3-15. This approach cuts the required shift register clocking rate by a factor of four.

Four video driver circuits are mounted on a pc-board along with two high speed sampling clock drivers. Two such pc-boards are paired to drive a single 176 conductor Kapton cable which is split to allow 88 conductors to be soldered to each pc-board.

3.5 Wafer Processing of the Medium Density Display

Initially, the seven-mask process sequence for the medium density display was thought to be fully developed, from previous LC/MOS display processing with a low density display (3.94 p/mm). Unfortunately, there developed several processing difficulties that occurred as a result from scaling the low density display layout, in Figure 3-10, to achieve the medium density display layout, in Figure 3-8. For instance, the etching of the "via" contacts for top reflector metal to contact

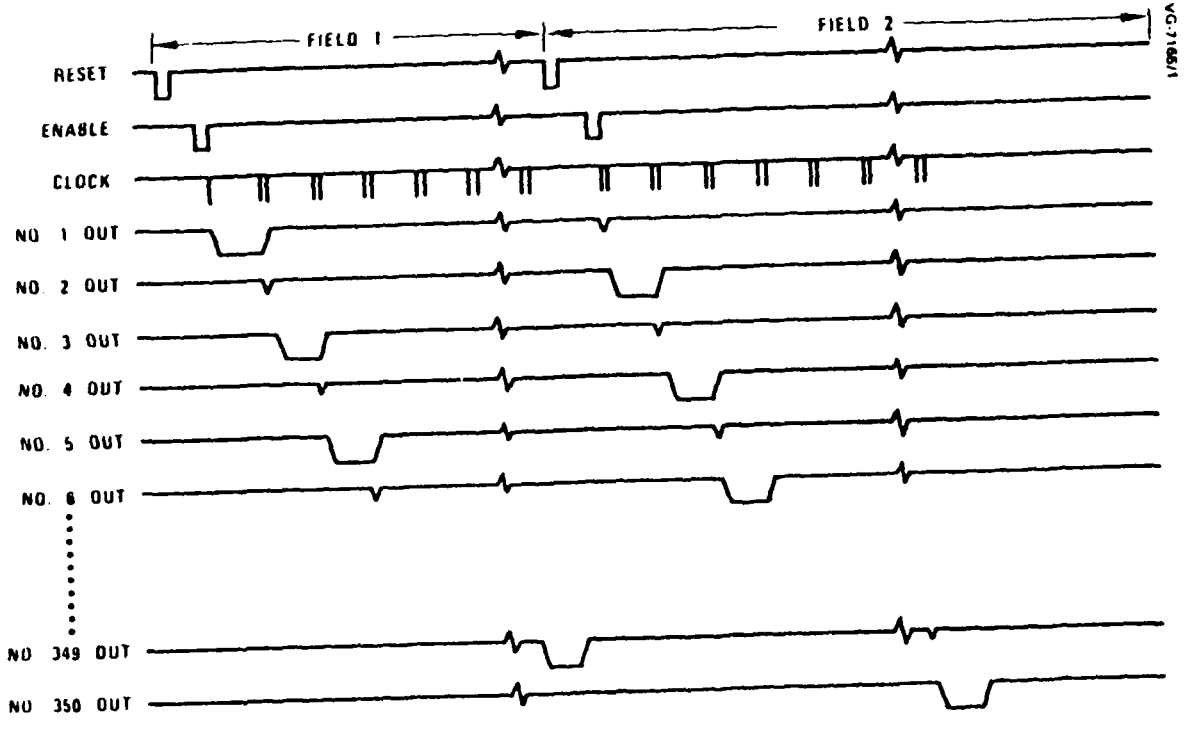
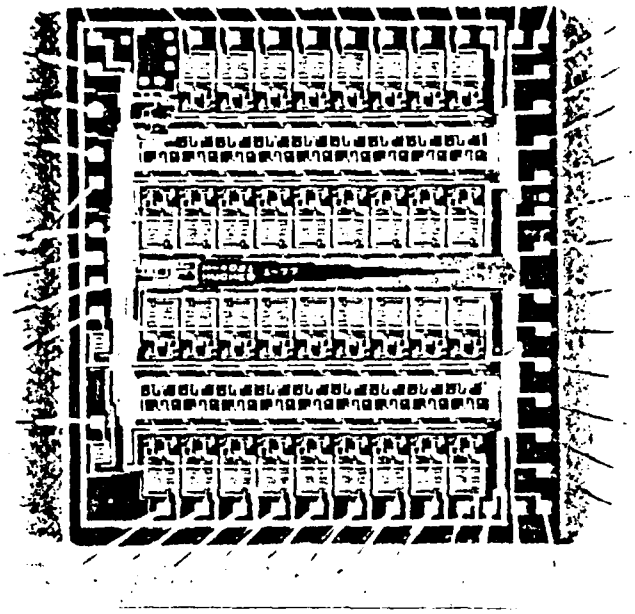
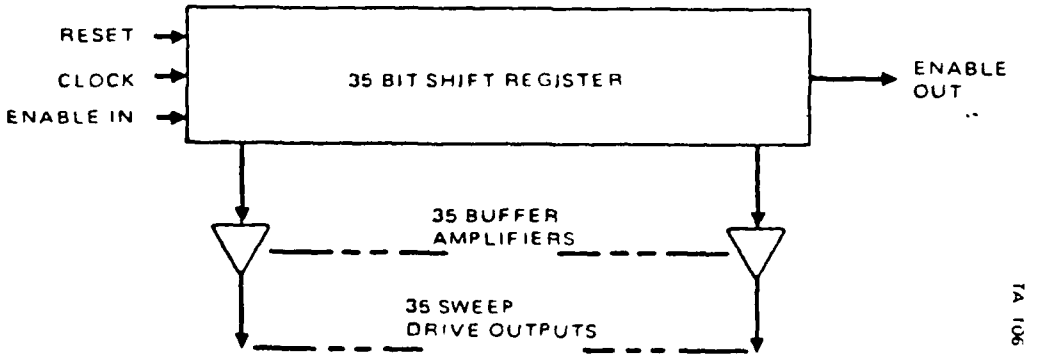


Figure 3-12. Discrete Gate Driver Circuit Timing Diagram for 525 Line TV Rates



Gate driver circuit layout



Gate driver circuit block diagram

Figure 3-11 H4021 Custom Integrated LC/MOS Gate Driver

Table 3-1. Liquid Crystal Display

Parameter	H4020 1.75" x 1.75" array 3.91 p/mm	H4030 .17"x .17" array 23.1 p/mm	H4035 .40" x .54" array 23.1 p/mm	H4080 .99"x.74" array 12.25 p/m
Display Size	4.44 x 4.44 cm	.43 x .43 cm	1.01 x 1.37 cm	2.91x2.27 cm
No. of pixels	30,625 (175x175)	10,000 (100 x 100)	74,880 (240x312)	76,800 (240 x 320)
Pixel storage capacitance	7.64pf	190ff	91.9ff	447ff
Average stored voltage (V_o = 20 volts)	15.1V*2	15.6V*2	13.9V*1	15.24 *1
Vertical drain line RC constant[3]	38 us	8 us	2 us	3.55 us
Horizontal gate line RC constant[3]	48 us	28 us	7 us	10.2 us

1 Display operated at std 525 line TV rate, over write fields onto display in 16.7 msec.

2 Display operated at std 525 line TV rate, interlaced fields onto display in 33.4 msec.

3 Line RC constant is time of signal propagation to 95 percent level.

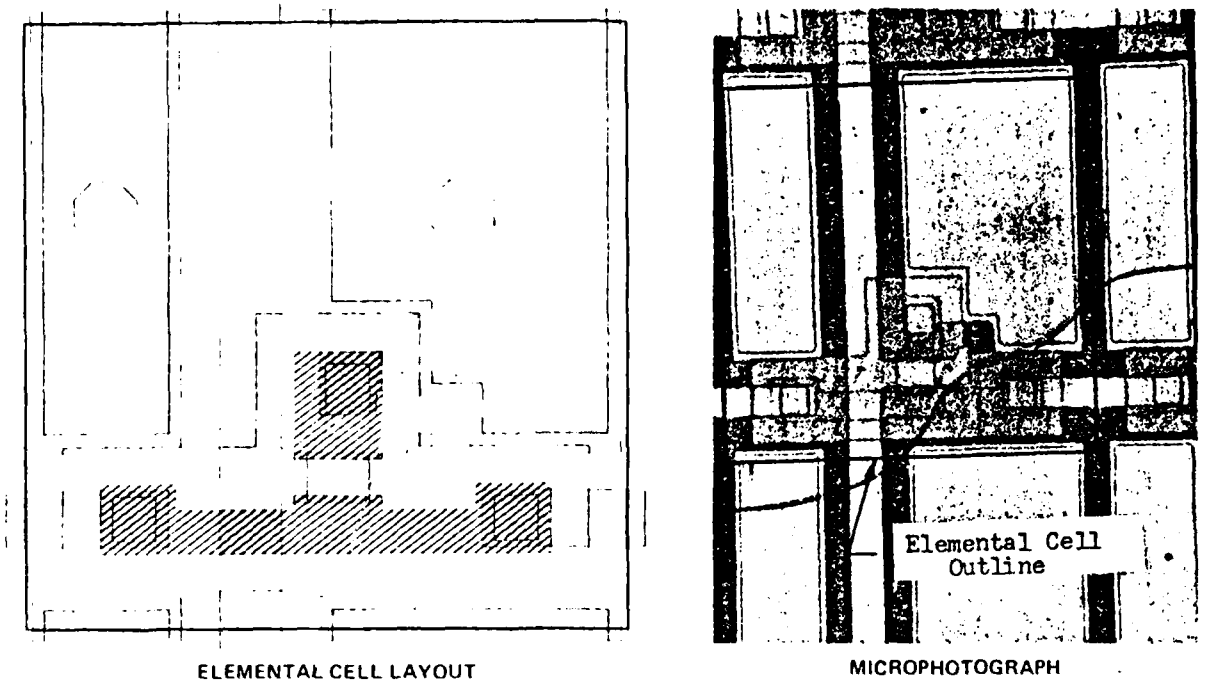


Figure 3- 10 Layout of the 3.94 p/mm Pixel Cell on the H4020
(1.75 in. x 1.75 in. Array for Integrated Head-up Display)

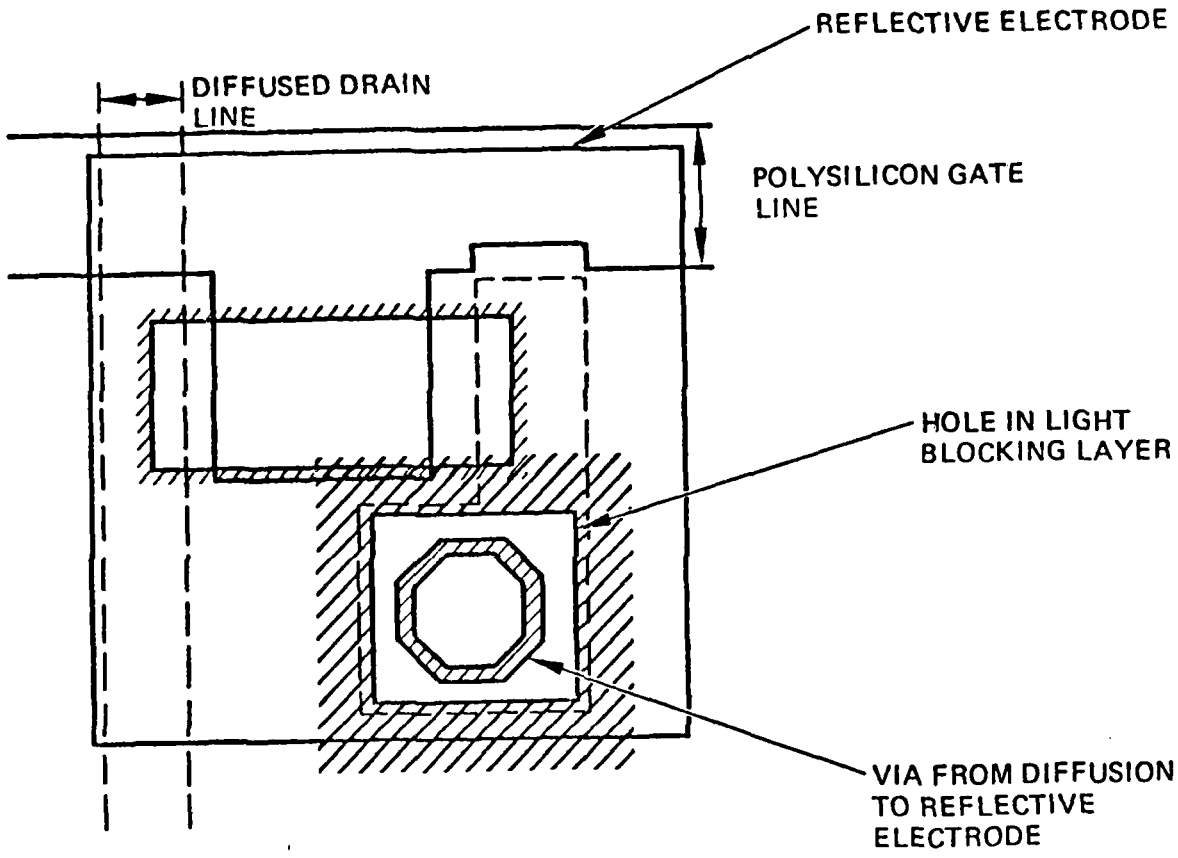


Figure 3-9 Layout of the 23.1 p/mm Pixel Cell on the H4035 (High Density Matrix)

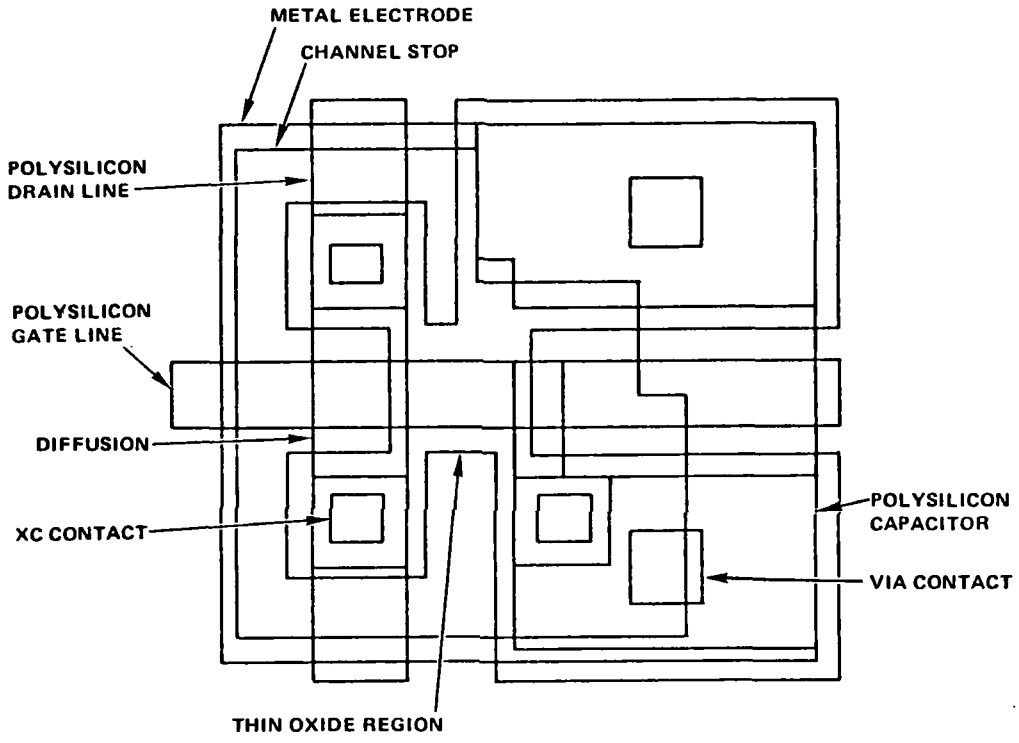


Figure 3-8 Layout of the 12.25 p/mm Pixel Cell on the Medium Density Display (H4080)

The medium density pixel design is shown in Figure 3-8. Earlier density pixel designs are shown in Figure 3-9 and 3-10. The lower density pixel designs operate on the same principles as described above. However, a significant difference between the high density pixel design and lower density pixel designs is the elimination of the phosphorous implant regions (known as field channel stop (CS)) in the high density pixel cell. Another significant difference is the vertical capacitor configuration, which incorporates its ground electrode as a light blocking layer (the buried metal layer) in each high density pixel cell. This light blocking layer prevents photons from generating electron-hole pairs which would interact with the video signals propagating on the drain lines and stored on the transistor source regions. The characteristics of these various pixel designs are shown in Table 3-1.

3.4.2 Drive Electronics Design

The drive electronics interface to the medium density display consisted of previously designed discrete driver circuits, established on the Air Force Integrated Head-Up Program for the low density matrix display. This first set of discrete driver circuits established the basic logic implementations and circuit concepts used in the subsequent integrated driver designs of the high density display. These discrete driver circuits were used to provide the appropriate signals to the center 175 by 175 pixel section on the medium density display, by using existing interconnect cables between the pc-boards and display carrier.

The discrete driver circuits consist of similar design types to those used in the high density display—gate driver circuits and drain driver circuits. The interconnection between these driver circuits and the medium density display are made with miniature cables utilizing 100 lines per inch densities. The timing characteristics are discussed in the following section for the discrete gate and drain driver circuits that were used with the medium density display.

3.4.3 Discrete Gate Driver Design

The discrete gate driver circuit, shown in Figure 3-11, consists of a thirty-five bit serial input shift register with thirty-five buffered parallel outputs. A delayed vertical sync pulse, shortened to one horizontal period in width, is applied to the Enable-In input. The circuit is clocked by horizontal sync, and successive lines on the display are enabled as the Enable-In pulse propagates from stage to stage in the shift register. The interlace required for compatibility with standard television inputs is accomplished using the timing shown in Figure 3-12. On the first line of field one, a single clock pulse is applied to enable the first output.

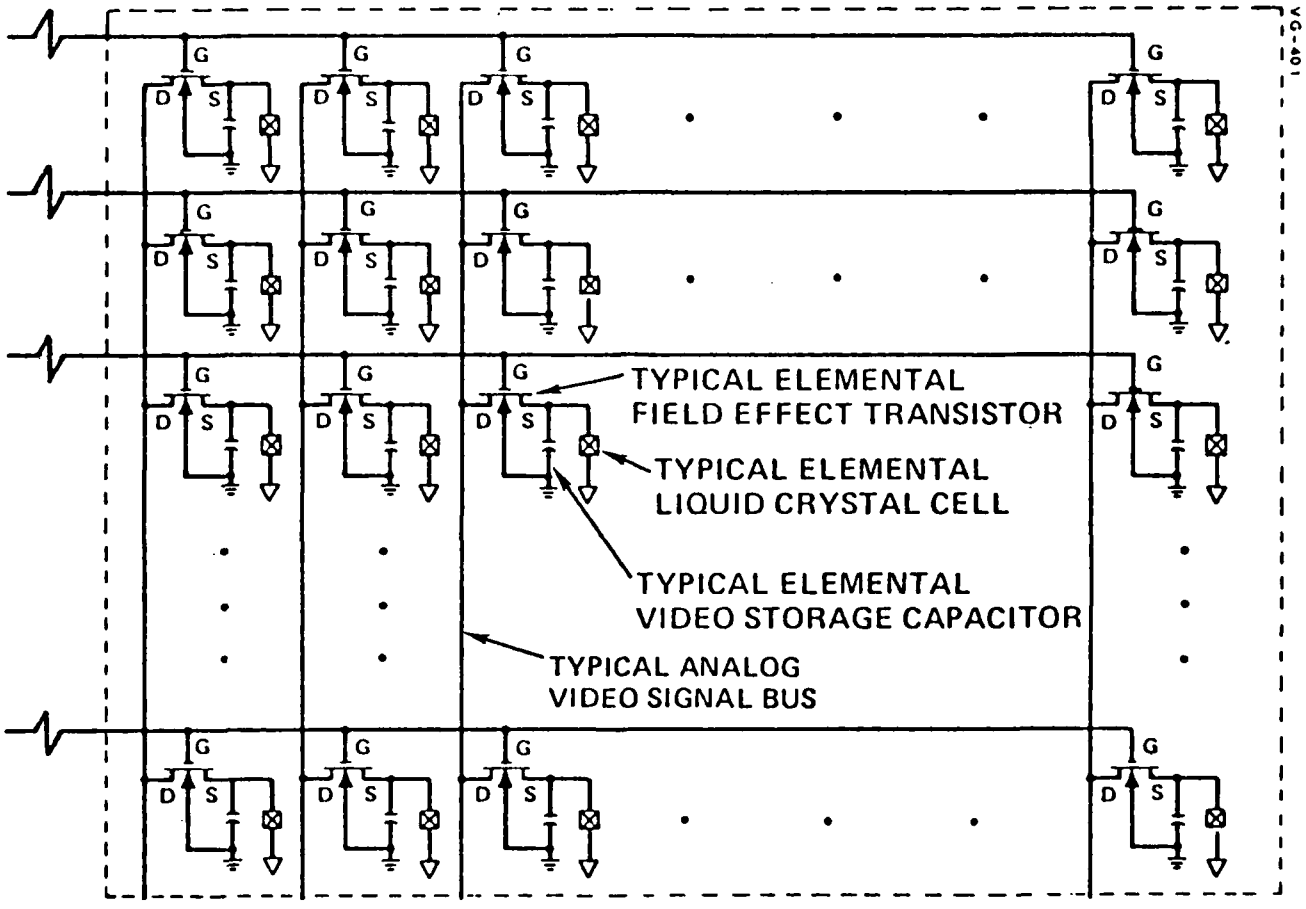


Figure 3-7. Medium Density (H4080) Matrix Array Schematic

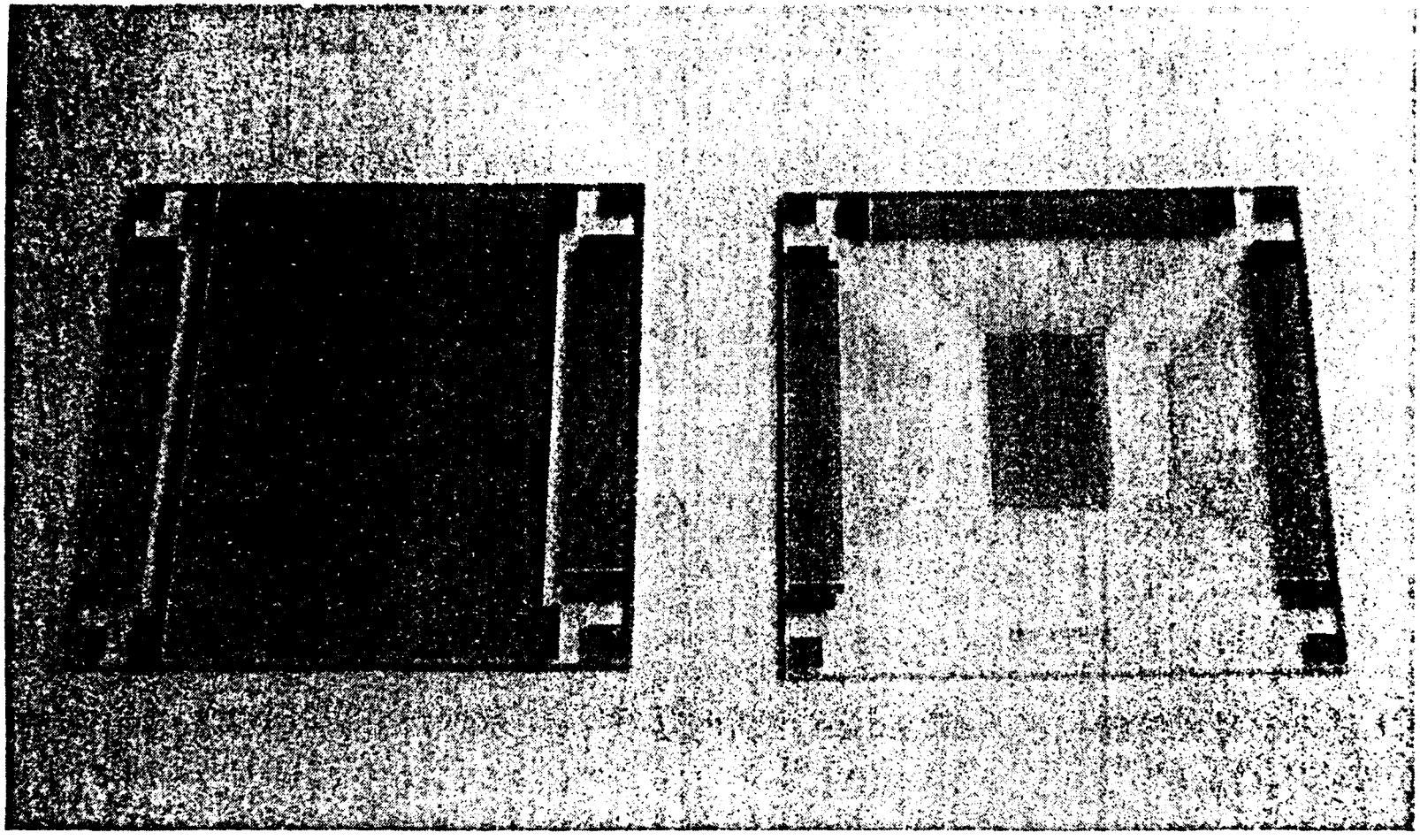


Figure 3-6. Comparison Between Low Density (left side) and Medium Density (right side) Pyrex Glass Circuit Plates

line interconnect, labeled in Figure 3-6, runs through the display mounting area in order that the display drain lines are driven from both ends. The gate line interconnect is positioned on both sides of the display in order that the display gates are driven from both ends.

Notice in Figure 3-6 that both types of circuit plates (H4020 and H4080) have their interconnect terminating at the plate edges with .010 inch line center spacings. Thus, the H4080 plate configuration interfaces to existing cables and drive electronics boards. In addition, the center 175 by 175 pixel area of the medium density display is wire bonded to the interconnect lines on the pyrex circuit plate.

3.4 Display and Driver Design

This subsection will cover the design of the medium density array and also the design of the discrete driver circuits used with it. A liquid crystal matrix display is not directly compatible with a standard television signal source any more than a CRT without its associated syncronization pulse detectors, deflection generators, and video amplifier. To drive a liquid crystal matrix display, additional components are needed in the form of display drivers, interface circuits, and high density connectors.

3.4.1 Design and Operation of the Array

The circuit schematic for the matrix array is shown in Figure 3-7, without drivers. The display is arranged with 320 horizontal pixels and 240 vertical pixels, and with a pixel density of 12.25 p/mm. The horizontal display lines address 320 pixel rows of MOS p-channel transistors. These transistors are activated by their gate electrode connection to the horizontal lines, when the operating voltage of -30 volts is applied, as referenced to the silicon substrate biased at ground. These horizontal lines are referred to as the gate display lines. The discrete driver circuits which provide the operating signals are called gate driver circuits. Each pixel transistor is used as a switch to charge a capacitor to a voltage determined by the video input signal. The vertical display lines are connected to the drain p^+ diffusions of the transistors in a column 240 transistors high. These lines provide the sampled video signal from the discrete driver circuits—called drain driver circuits. The video signal levels are typically between -20 volts to 0.0 volts on these lines. The video signals from the vertical drain lines provide the charge to the pixel storage capacitor in those elements selected by a horizontal gate line activating the transistor.

The capacitor holds the voltage on the liquid crys' which controls the amount of light scattered by the liquid crystal. The storage capacitor charge provides the voltage potential and supplies the direct current across the liquid crystal material to the conductive layer on the top plate glass, also biased at ground.

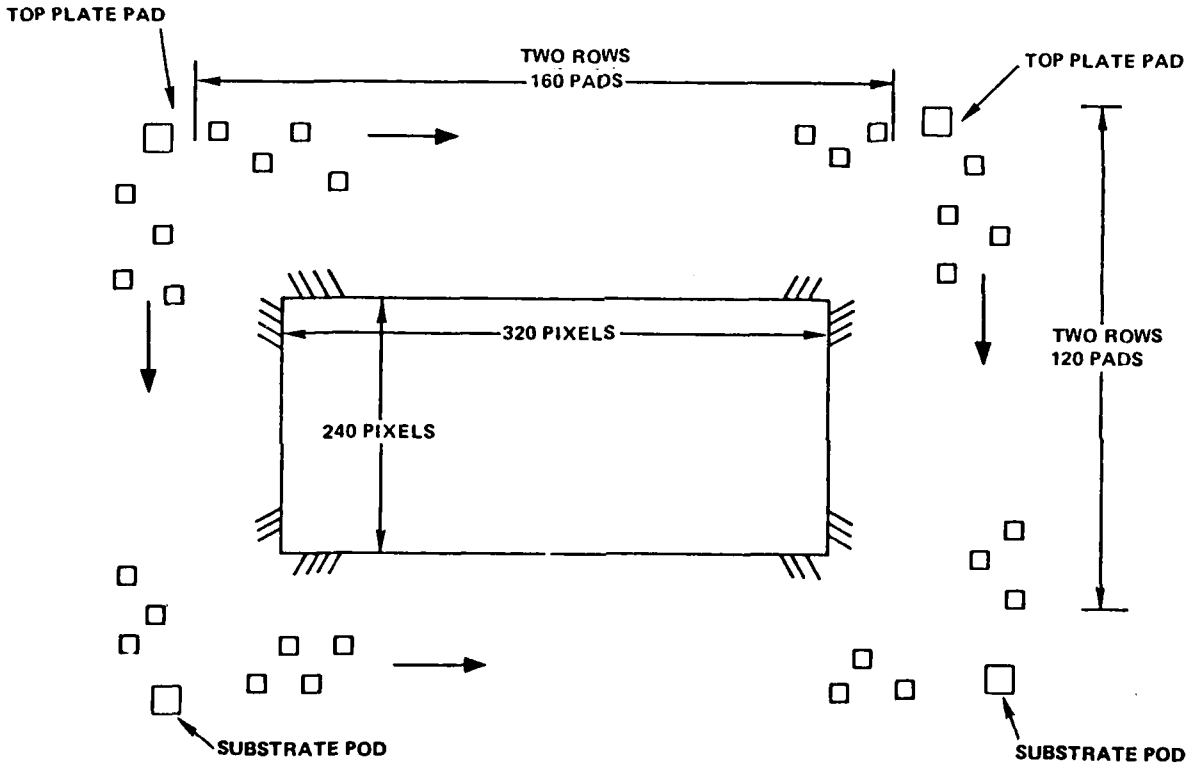


Figure 3-5. Medium Density Display Layout for H4080 Display

MOS chip to a gold pattern on a glass plate.

Results of the bonding study can be summarized by these observations: the Al to Al bonds between MOS chips have highest bond continuity yield; the CrNiAg to Au bonds between MOS chip and glass plate have highest bond position yield; the average bond pull strengths were slightly higher for CrNiAg (10.3 grams) than for Al (9.5 grams) bond pads. By comparison to our 1.75" liquid crystal display, the higher density bonding will reduce, approximately by 10%, the present yield typically encountered at the .010 inch center to center bond pad spacing. However, the yield of the higher density bonding is expected to improve with experienced personnel and automatic techniques.

The results of the bonding study were incorporated into the medium density display as .0035 inch bonding pad center spacings. This spacing will allow for the redundant drive of all interconnect lines. By merely extending existing low density (3.94 p/mm) bonding techniques to the medium density display, we are able to interconnect the center 175 by 175 pixel area with existing interconnect cables and drivers. We used .001 inch aluminum wire to bond between CrNiAg on the LC/MOS display and CrAu on the glass circuit plates.

3.2 Evaluation of the Medium Density Display Design

After an evaluation of the wire bonding capabilities from presently available bonding equipment, the medium density display cell and bonding pad concepts were defined and the display configuration was finalized. Several of the significant layout characteristics are described and illustrated in Figure 3-5. All the interconnect lines are brought out to pads, to provide for redundantly driving each line with wire bonds to the glass circuit plate. The actual display area is 18.96 mm by 25.28 mm. The pixel dimensions have all been scaled down from an earlier 3.94 p/mm liquid crystal display. The medium density display (12.25 p/mm) utilizes the fully-developed seven-mask MOS process for our 3.94 p/mm display. The medium density display design, layout, and photomasks were developed on this program. The resulting display layout provided for the positioning of four die on one 3 inch silicon wafer.

It is recognized that a 240 by 320 display does not provide a full TV standard raster; the resultant being 1/4 of such a display. Nevertheless, the medium density display implemented in this contract does represent a significant milestone on the road to an integrated full 525 line TV capability.

3.3 Design and Fabrication of the Circuit Plate

In this task a pyrex circuit plate was designed and fabricated that allowed the interfacing of the medium density display to the existing set of interconnect cables. The interconnect line layout provides for the redundant drive of the display lines by the existing cables. For instance, the drain

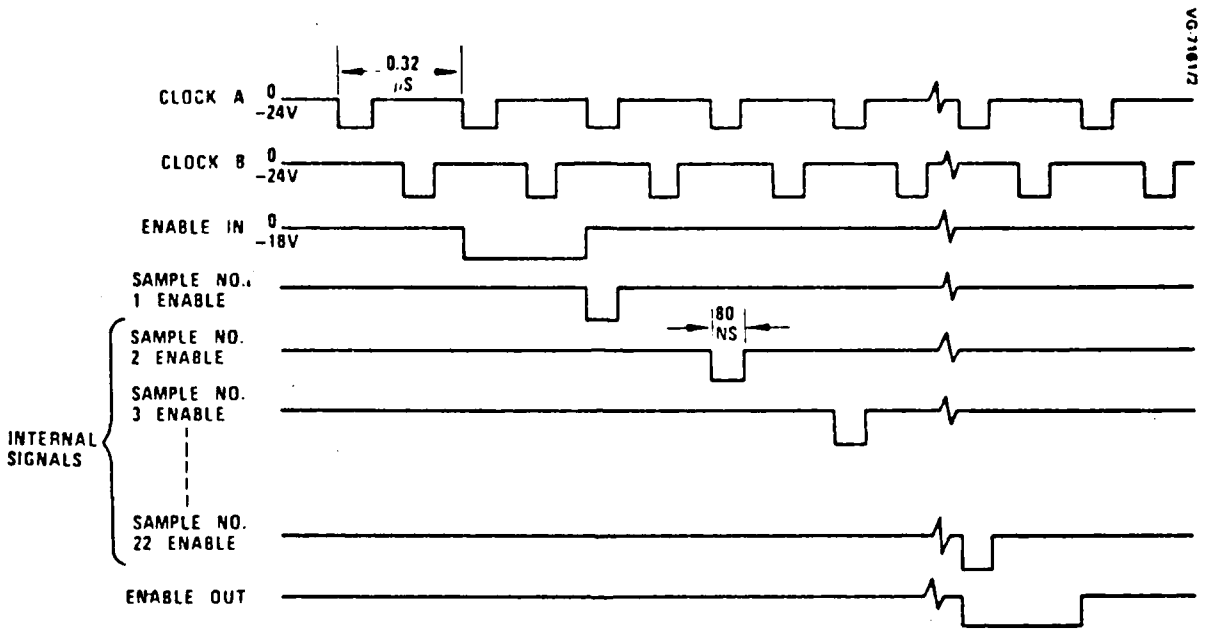


Figure 3-14 Discrete Drain Driver Circuit Timing Diagram for 525 Line TV Rates

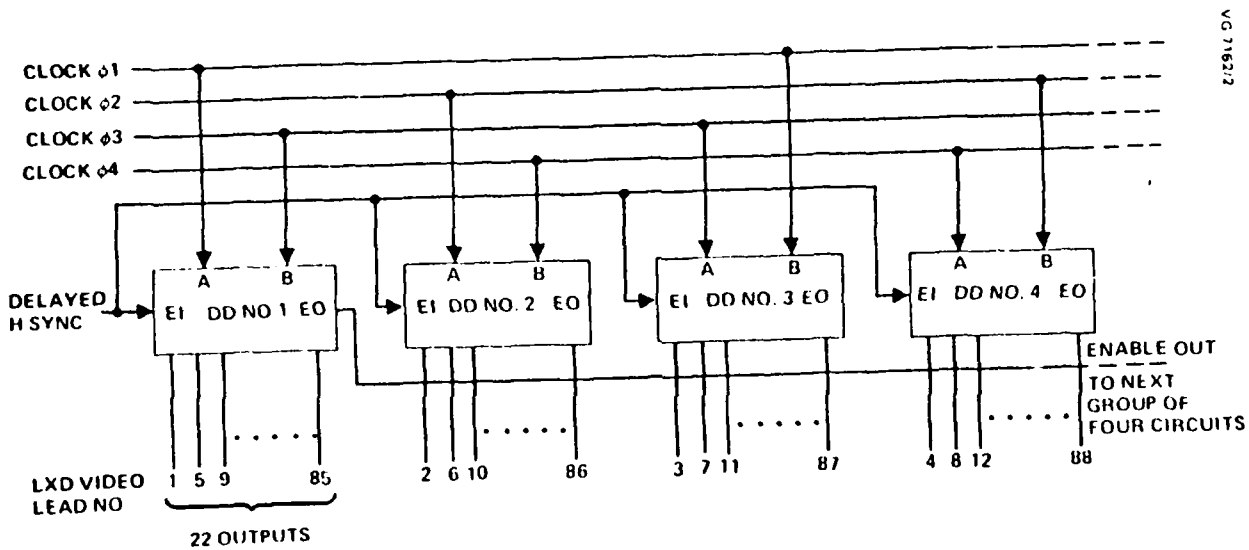


Figure 3 - 15 Discrete Drain Driver Circuit Interfacing Configuration

the polysilicon capacitor shapes caused a metal step coverage problem. The patterning of the smoothing material over the medium density display resulted in "unsmoothed" display surfaces. The surface area of the pixel edges and via side-walls resulted in more random surface reflections than occurred from a "smoothed" low density display. In addition, the medium density display exhibited a light sensitivity to illuminations above 300 foot-candles.

In developing the solutions to the medium density display process, tests of individual process steps were carried out, especially with the light blocking layer and insulating dielectric/smoothing layer. For instance, tests were conducted to develop the light blocking layer material (buried metal layer) which was deposited between the polysilicon interconnect layer and the top reflective metal electrode. This light blocking layer prevents photons from generating electron-hole pairs which would interact with the video signals propogating on the drain lines and stored on the transistor source regions. The smaller, scaled distances in the medium density display cause the source-drain regions to be more susceptible to photon generation, than in the low density display with larger (X10) separations between the source drain regions. The primary metal utilized was an aluminum-silicon alloy. This alloy minimized hillock projections which protruded upward, possibly shorting to the top reflector electrode. Next, tests were run to develop an intermediate insulator layer between the polysilicon interconnect-buried metal and reflective electrode buried metal layers, as shown in Figure 2-8. This intermediate insulator was to also serve as the smoothing material that would enable the display surface to achieve the necessary optical flatness quality, without the objectionable pixel surface edges. The basic material used in these experiments was a polyimide film, PIQ-13, from Hitachi Corporation. A large development effort was expended on this program, and on Hughes IR&D, to determine the processing techniques for achieving a non-light-sensitive, "smoothed" medium density display.

There were six wafer lots processed through the various steps of the semi-conductor processing flow chart shown in Figure 3-16. The average throughput of a wafer lot to the polysilicon test point was thirteen weeks. The evaluation of the wafer lots at intermediate test points provided the necessary feedback in optimizing the performance of the medium density displays for the feasibility modules. For instance, the evaluation of test wafer lots and display characterization provided the necessary information to direct the process modifications for achieving the desired properties in the insulating dielectric layer which also served to smooth the display surface.

A line defect-free medium density display was demonstrated from a wafer processed in the second wafer lot. However, this display exhibited light sensitivity, as did all the display wafers processed for this program. The feasibility modules were processed up to the polysilicon test point on this program. Then, these display wafers were processed

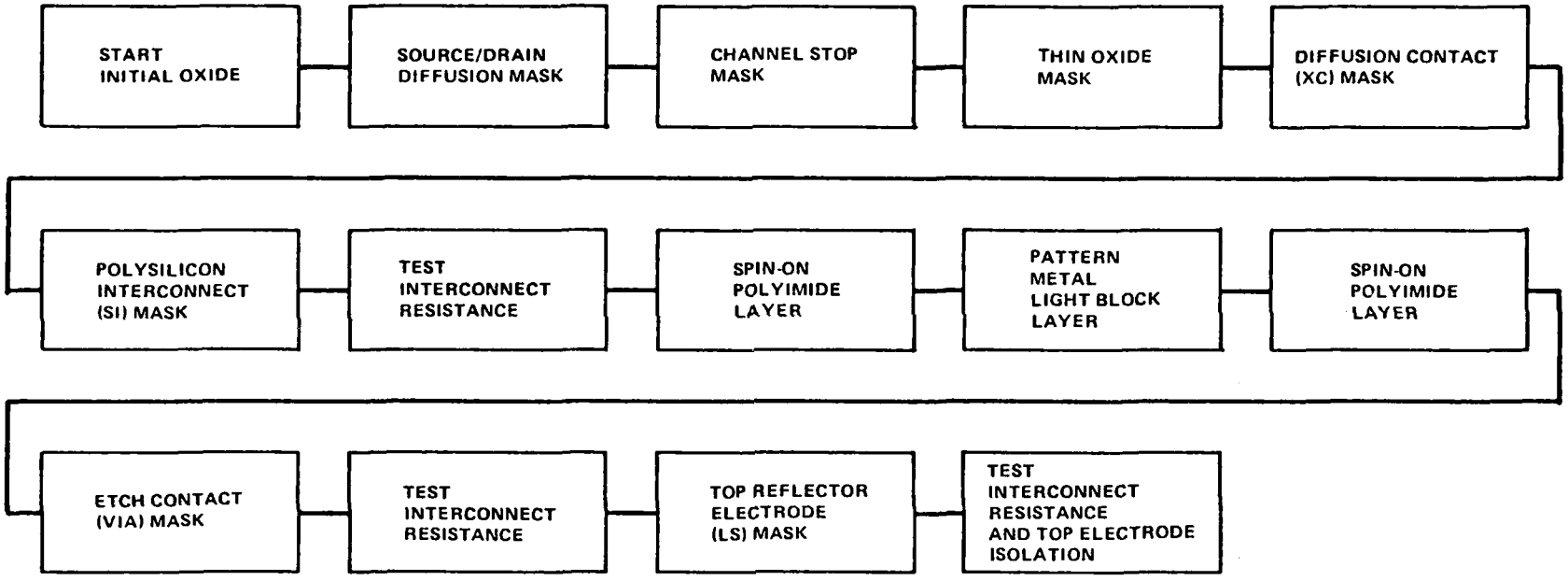


Figure 3-16 Medium Density Matrix Display Process Flow Chart

on Hughes IR&D funds through the newly developed polyimide smoothing process and top reflective electrode metalization. These subsequent process steps past the polysilicon layer incorporate a light block layer over the display area to prohibit the generation of photons which degrade the video signals on the drain lines and pixel storage capacitors.

A certain degree of success was achieved in developing solutions to the initial process difficulties with the medium density display. The demonstrated performance of the four feasibility modules alludes to the accomplishments in processing development. Several recommendations concerning additional application and process refinements are made in the conclusions portion of this report.

3.6 Description of the Liquid Crystal Material

The liquid crystal material that was used in this program is a Hughes proprietary mixture (2N40 mixture) which consists of six ester-based components with a negative dielectric anisotropy. A general description of liquid crystal materials is given in Appendix A. The nematic range of 2N40 mixture is between 14° C and 59°C. For long life in a DC dynamic scattering operational mode the 2N40 mixture is doped with a non-conductive redox pair Dibutylferrocene (DBF) and Trinitro-9 Fluorenylidene Malononitrile (TFM) as the donor and the acceptor pair, respectively. These redox pairs in highly purified 2N40 mixture can readily undergo reversible reduction and oxidation reactions at much lower potentials than the liquid crystal material itself. The addition of these dopants therefore determines the conductivity and controls the electrochemical reversibility of the system. The percentage added is adjusted to provide optimum dynamic scattering contrast with an applied D.C. potential. Such dopants provide the basis for long lifetime DC dynamic scattering effects.

Figure 3-17 shows the scattering data for the 2N40 mixture. Full scattering is obtained at an 18v bias. A gentle slope at voltages less than 12 volts is desirable for obtaining the optimum numbers of gray shades. The maximum contrast ratio of a TV display with a silver reflector has been measured at 20:1. This is based on the measurement set up with a point light source at the angle appropriate for maximum contrast. This contrast will easily provide the desired number of 2 luminance steps. Life test data of a DC operated dynamic scattering display is shown in Figure 3-18.

3.7 Testing of the Medium Density Display and Drivers

Several device monitor structures were incorporated on the same wafer around the medium density display for in-process evaluations (i.e., transistor threshold). In addition, process parameters were monitored by the insertion of blank test wafers at such process steps as furnace

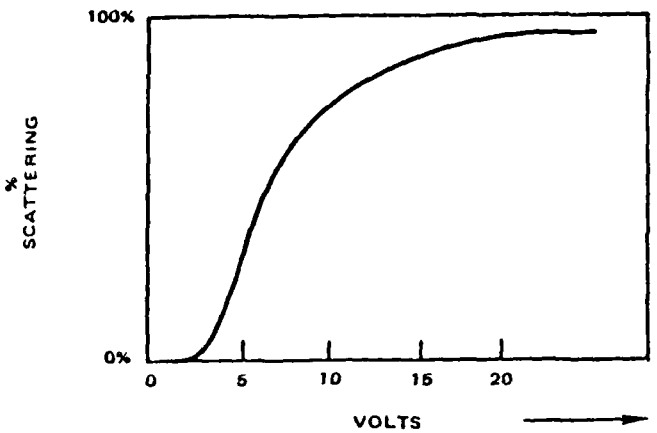


Figure 3-17. Scattering Versus Voltage of 2N40 Liquid Crystal Material

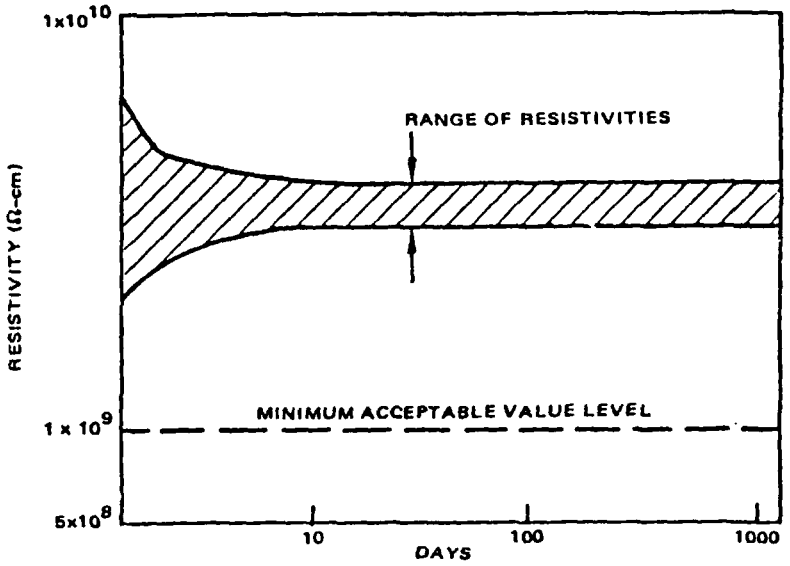


Figure 3-18 Life Test Data for 2N40 Liquid Crystal Cells at Constant Voltage (20V) Operation

diffusions, implantations, gate oxide growth, and deposition of interconnect layers. These process-parametric test wafers provided for the complete characterization of the medium density display processing

Test points were included at the ends of each display line. This permitted automatic computer testing to be used to collect information on the medium density display line defects. This information analysis quickly confirmed that the medium density display photomask set was relatively free of line defects in the center 175 by 175 pixel area used to demonstrate feasibility for this program. However, there were found to be two mask related line defects on two of the four die. Both these line defects were located outside the center 175 by 175 pixel area activated in the feasibility models.

The tests which were run on each line of each display check continuity of the line as well as whether the line is shorted to substrate at an applied potential of -20 volts relative to substrate. These tests, developed for use originally on lower density (3.94p/mm) displays and adapted for use on the higher density display developed during this program, have been proven to do an effective job of identifying most line defects which affect final display performance.

The discrete driver circuits are functionally tested following processing using the electroglas probe station, various signal generators and power supplies to generate inputs to the die under test, and an oscilloscope to check the die outputs for proper performance. Each device is retested after it has been sawed out of the wafer, mounted into a package, and wirebonded to the package leads. A final test is perfonned after the package is sealed.

The drain driver packages undergo further testing to determine their output drive voltage vs input video voltage characteristics. Only devices with very similar characteristics are used in any one system. This is necessary to avoid striping of the display image due to uneven device performance. It is noteworthy that the integrated drain devices developed for the high density display had this problem designed out of them, and in fact did give very uniform performance.

3.8 Packaging of the Medium Density Display and Drivers

The medium density display utilized the same cell assembly techniques as developed earlier for previous low density displays. For instance, the mylar spacer placed between the top glass plate and the silicon display was 12 microns thick. Six medium density displays were fabricated for this program. However, additional display fabrication was placed on hold until the development of nonlight sensitive display wafers. The recent achievement of the medium density displays, which are not light sensitive, provided several display wafers which were fabricated into feasibility modules. An assembly process flow chart that illustrates each step through the assembly process is shown in Appendix D.

The devices used to drive the medium density display were processed separately from that display. The devices are tested and then packaged into standard ceramic 40 or 48 pin packages using standard semiconductor processes. Specifically each die is mounted in the package cavity with conductive epoxy and wirebonded to the package leads using aluminum wire. After testing the packages are sealed by affixing lids, again using conductive epoxy.

4.0 THE PROGRAM - TASK BY TASK

This section summarizes the work performed as it relates to the nine tasks detailed in the proposal. It is not meant as a detailed list of accomplishments; rather it is hoped that it will serve as a review of the previous sections. It also contains information on the hardware (the proof-of-progress breadboard and the feasibility modules with their associated electronics) which was delivered during the course of the program.

4.1 Optimization of Processing

A great deal of process optimization was required during the course of this program. The high density display integrated drivers were successfully fabricated and the designs proven. This included the development and implementation of a high value resistor structure. Problems developed due primarily to the low integrity obtained in the thin (3000A) insulating layers used to separate the light blocking layer from other metal layers.

The medium density display required optimization as well, despite its design being similar to the one used most successfully in the past. Fabricated devices proved light sensitive and required the development of a light blocking layer, done on subsequent IRD, to yield light insensitive devices. This effort proved successful, and several light insensitive displays were delivered as feasibility modules.

4.2 Wafer Production

Twelve lots of high density displays with integrated drivers were started. Two of these lots are presently unfinished as they were in process when the program was redirected.

Six lots of medium density displays were processed. These lots provided all of the devices used in the delivered displays.

4.3 Cell Assembly Techniques Development

Cell assembly techniques for the high density display were developed on this program. These provide for mounting of the display on a molybdynum heat sink which is then mounted onto the ceramic card used for the leadout and pins. The card plugs into zero insertion force sockets on the front of the display interface electronics box. The package handles the display heat load without allowing the liquid crystal temperature to rise above its clearpoint.

Cell assembly techniques developed for the medium density display relate to the wirebonding of the display to the circuit plate at .0035 inch wirebond spacing. The other assembly procedures used on this display were developed previously.

4.4 The Proof-of-Progress Breadboard

The object of this breadboard was to demonstrate and deliver a LC/MOS matrix display feasibility model showing the viability of the higher density design (greater than 3.94 p/mm) and the anticipated appearance of the feasibility module.

Fabrication of the high density display as a proof-of-progress breadboard was never accomplished as a result of the inter-layer shorting in the matrix array between top reflector electrodes and the under lying light block layer. After the Tri Service committee redirected the program efforts, the proof-of-progress breadboard was successfully demonstrated and delivered.

The proof-of-progress breadboard was demonstrated to the Tri Service representatives on October 27, 1980. This medium density display was line-defect free, but exhibited a light sensitivity problem. Another display, fabricated in the same manner, was delivered as the proof-of-progress breadboard for this program. The demonstration of the proof-of-progress breadboard was performed on one of the electronics boxes that were delivered on this program. Each box included the driver circuits, boards, and cables for interfacing with the medium density display.

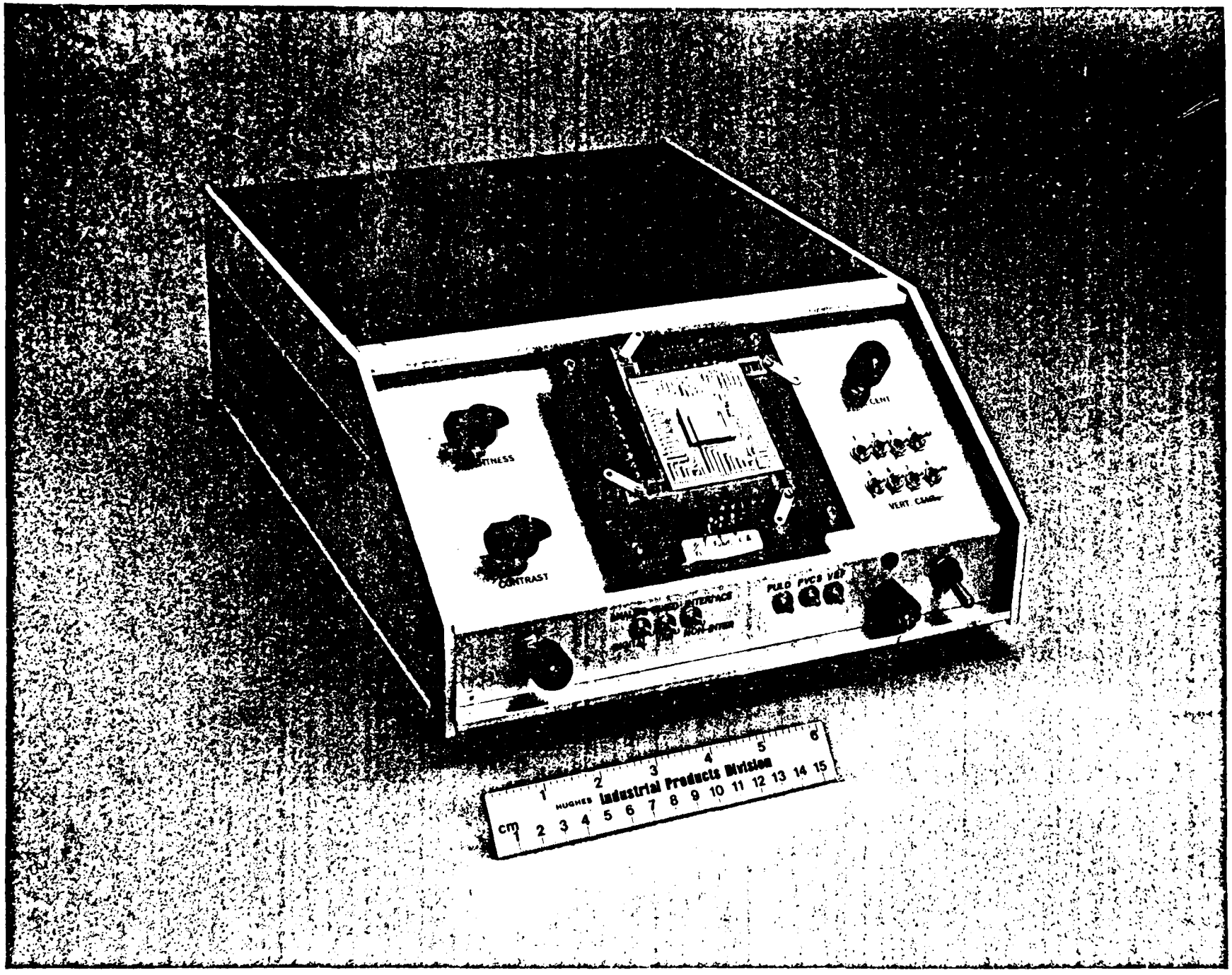
4.5 Interface and Display System Techniques Development

The object of this task consisted of defining the interconnection scheme between the high density display and the peripheral electronics, the design and fabrication of the peripheral electronics, and the fabrication and packaging of the display system. A major part of this task was to be the incorporation of lighting into the electronics system in accordance with the program goals for luminance uniformity.

Two electronics boxes designed to drive the high density display with integrated drivers have been built and checked out as operational with functional integrated driver circuts. An electronics box is shown in Figure 4-1. The interfacing of the peripheral electronics (including incoming signal stripping and video multiplexing) to the high density display packaging scheme is via feed-thru pins located on the alumina substrate, shown in Figure 4-2. These feed-thru pins connect to zero-insertion sockets located on the front panel of the electronics boxes.

The application of a wedge lighting scheme was evaluated at the Hughes El Segundo facility, for implementation in this program. However, further development of a wedge illumination scheme was placed on hold after the redirection of this program's efforts by the Tri Service Committee.

Three electronics boxes were built to provide the video signals to the medium density display package. An additional set of spare drain driver circuits, boards and cables were supplied as backup to the electronics boxes. The electronics box, shown in Figure 4-3, accepts 525-line composite TV and provides the video signal to the LC/MOS display via the kapton cables that were designed for the IHUD, low density LC/MOS display. Both the electronics box design and driver circuit boards are extensions of a demonstration display unit that Hughes has been using for several years.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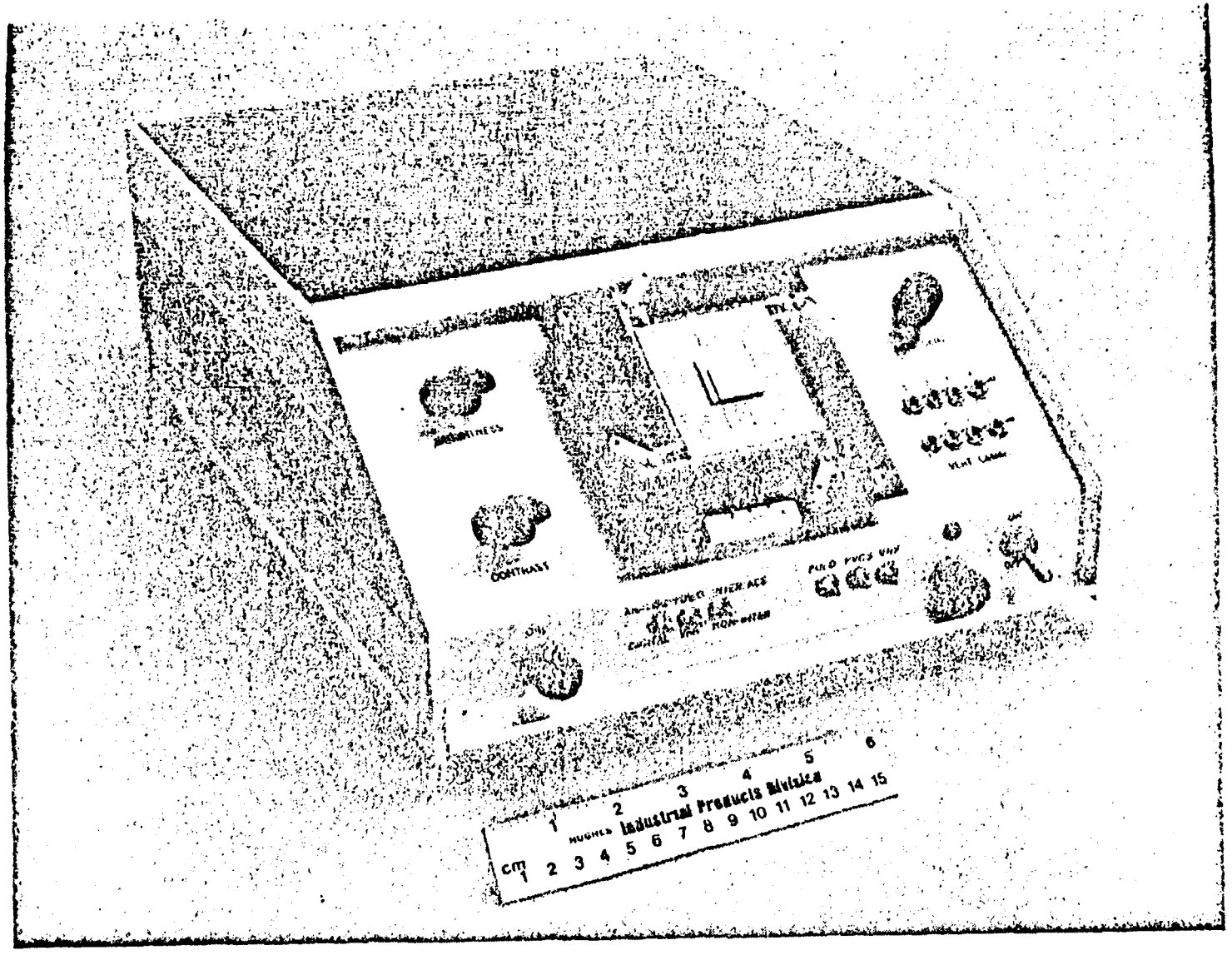
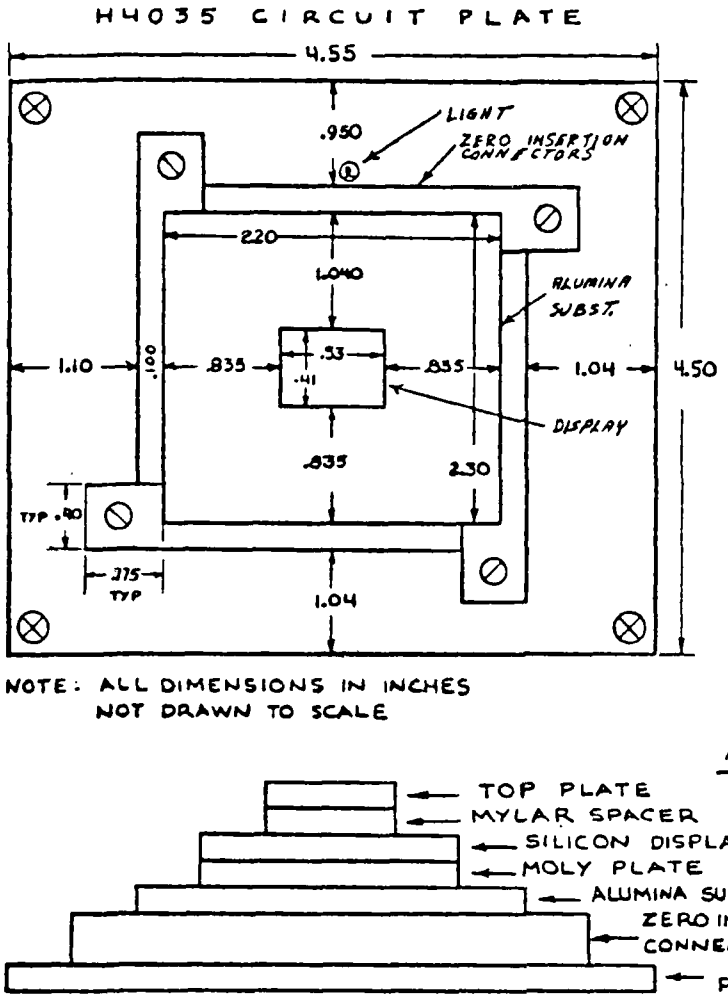


Figure 4-1. Electronics Box Module for Driving the High Density Display



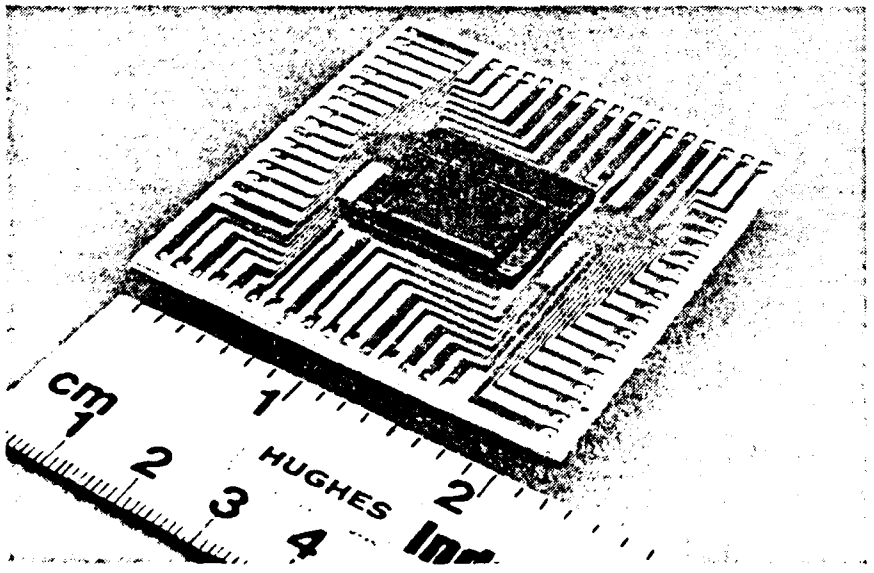


Figure 4-2 High Density Display Assembly Configuration

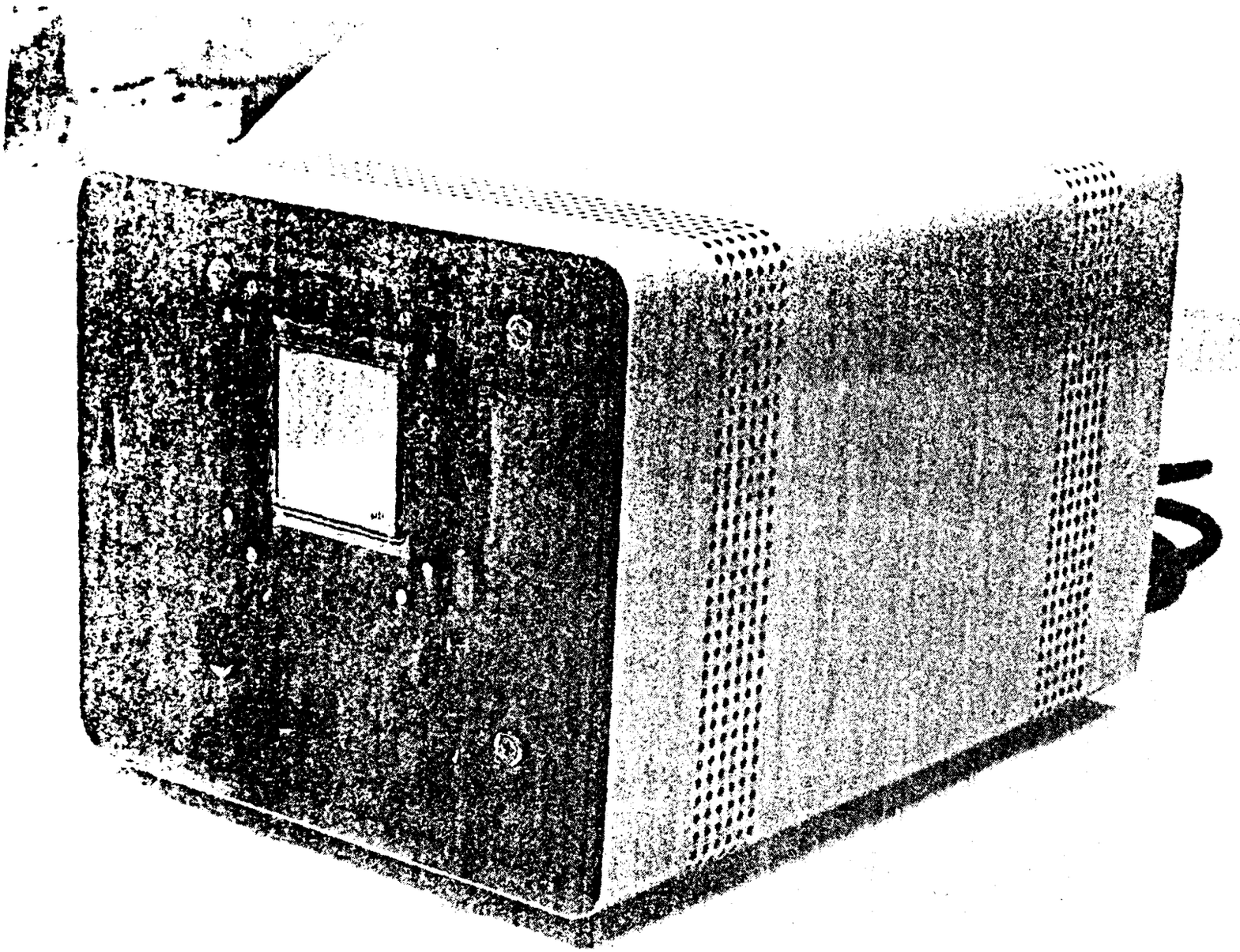


Figure 4-3 Electronics Box Module for Driving the Medium Density Display

4.6 Test Equipment Development, Evaluation of Wafer Lots

The object of these tasks consisted of testing the liquid crystal displays with a computer-controlled automatic probe station and custom designed wafer probe card. Extensive engineering evaluation in a manual mode, on the Electroglas probe station, was a large portion of this task during the initial wafer lot evaluations.

The implementation of a computer-controlled signal switching system was accomplished by programming the proper timing sequences into our Hewlett-Packard computer (Model No. 21 MX, Series E) and Matrix-switch (custom built switching relay system). Thus, the Matrix-switch enabled rapid variation of the input signals and the output signal analysis by computer-controlling the signal switching. This test sequence provided for the electrical characterization of the high density display interconnect lines (both gate and drain lines) for detecting any photomask-related line defects (either opens or shorts). The necessary wafer probe cards, engineering probe stations, electronics boxes, and computer-controlled switching capabilities were established for testing the high density lots on this program, and this sequence in the fabrication cycle is illustrated in Figure 2-7 and Figure 2-12. Step-by-step testing provided confirmation of the display's integrity prior to commitment to final package mounting and the application of the liquid crystal.

The existing computer controlled switching system and Electroglas probe station were readily adaptable to testing the medium density display at the various test points shown in Figure 3-16. For instance, the electrical tests provided information on gate and drain line resistances, interconnect line to substrate breakdown voltages, drain line contact resistance between polysilicon to boron diffused under passes, top reflector metal contact to the pixel storage capacitor, adjacent pixel to pixel leakage currents, and isolation of the bonding pads for the top cover glass from the silicon substrate.

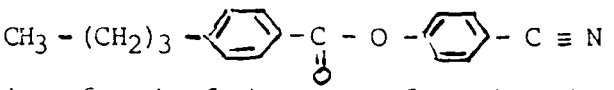
4.7 Assembly of Four Feasibility Modules

The objects of this task were to apply the assembly techniques developed for the proof-of-progress breadboard to the construction of deliverable displays, interface the display with separately evaluated signal processing electronics, and to fabricate the feasibility module display system.

Unfortunately, the development of a functional high density display was not realized on this program. Consequently, the Tri Service committee redirected this program effort to the development of a medium density display.

The assembly techniques which were used to demonstrate a line-defect free display, were also used to assemble the four feasibility modules for this program. The assembly run sheet, shown in Appendix D, was adhered to in the assembly of the four feasibility modules. Three feasibility modules were mounted into the three electronics boxes. Next, the operating voltages were adjusted in the drive electronics to optimize the video picture on the display module. The electronics boxes rely on ambient room lighting to illuminate the display module; no internal light source was included.

In general, when $\Delta\epsilon$ is positive, the molecular axis aligns roughly in the direction of an electric or magnetic field, whereas when $\Delta\epsilon$ is negative, the molecules orient themselves at an angle roughly perpendicular to the field. For the molecules of the LX substances used for airborne displays, only the electric field strength is of interest. The dielectric anisotropy is a function of the vector sum of the dipolar groups in the molecule. To prepare an LX with a strongly positive $\Delta\epsilon$, for example, it is conventional to to introduce the strongly dipolar nitrile group at the end of the long axis of the molecule, as in:



Individual properties of each of the types of LXs have been utilized in making displays. The properties associated with each type of LX material are listed below.

NEMATICS:	Dynamic scattering field effects (1) Twisted Nematic (2) Birefringent color switch (3) Nematic dichroic dye interaction
CHOLESTERICS:	Reflective color displays (1) Temperature sensitive (2) Pressure sensitive (3) Chemical vapor sensitive (4) Electric field sensitive
SMECTICS:	Thermo-optic storage display
HYBRIDS:	Thermo-optic Cholesteric-nematic phase change

A1.1 Dynamic Scattering Mode (DSM)

Briefly DSM may be characterized by electrical current-field induced hydrodynamic motion. Nematic LXs are optically anisotropic (i.e., they have different refractive indices for directions parallel to and perpendicular to the long axes of the molecules.) The effect of applying a voltage to and passing a current through a typical LX cell (see Figure A-2) is to disrupt the normally uniform molecular orientation in favor of a large number of small regions (domains) whose molecular orientation is different from those of their neighboring domains. The effect on light passing through the cell is that of closely spaced refractive index boundaries. These index boundries refract the light at various angles (i.e., scatter it). The result is a system that is optically homogeneous and transparent when no voltage is applied and highly diffusing or scattering when voltage is applied.

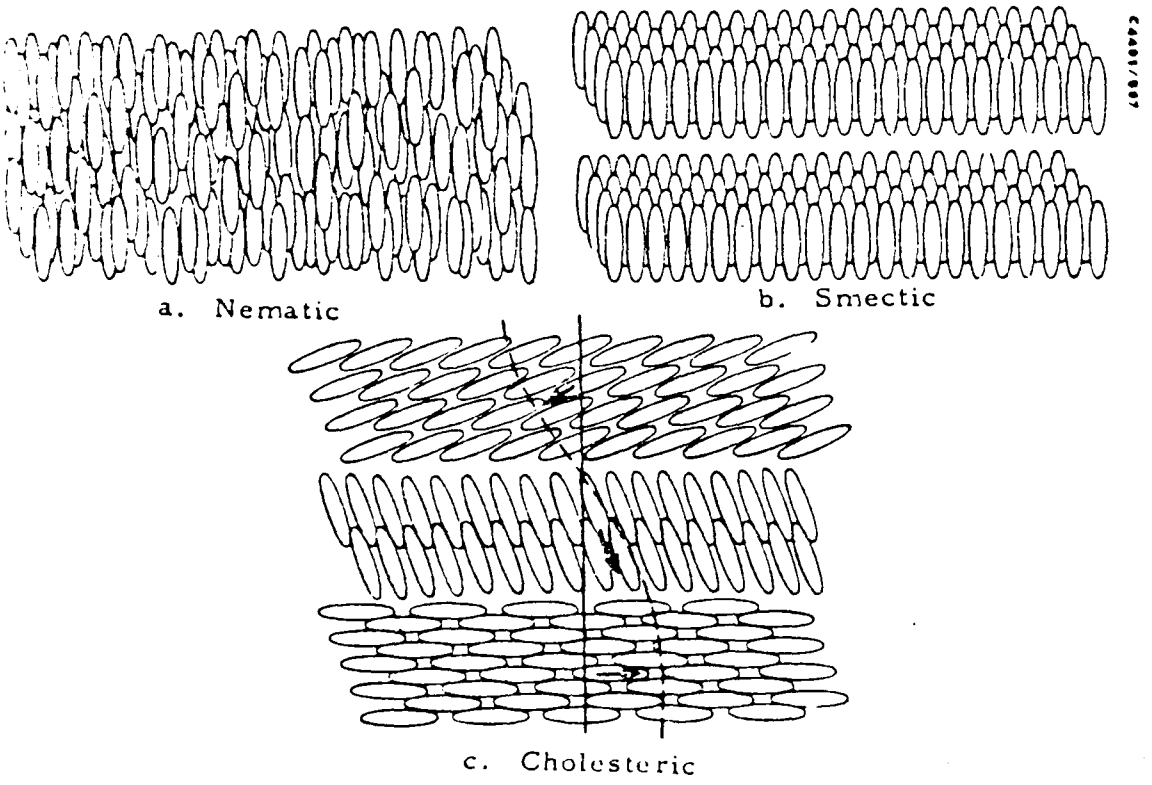


Figure A-1. Diagrams of packing effects in liquid crystals.

INTRODUCTION

Liquid Crystals (LXs) are organic substances which act like liquids over a specific range of temperature, while retaining some properties of crystals. Below the liquid crystal temperature range, the material becomes solid; above this range, it loses its crystalline properties and behaves like a true liquid. In the intermediate LX range, however, it passes through a turbid liquid state, which is termed the mesomorphic or "liquid crystal" state. The molecular arrangement in the liquid crystal state is more orderly than in the liquid state but less orderly than in the solid state.

The temperature range for the liquid crystal state varies with liquid crystal materials, and considerable effort has been devoted to developing materials which have liquid crystal properties over a wide range of temperatures, including normal room temperature.

Liquid crystals have been classified in three basic categories: nematic, smectic, and cholesteric. The terms denote characteristic spatial configurations assumed by the molecules of these materials. While the molecules of cholesteric LXs are optically active, those of nematic and smectic LXs are generally optically inactive, (i.e., they do not rotate polarized light).

Nematic LXs consist of rod-like molecules aligned in parallel, similar to matches in a box; it is this type of material that is presently used in the Hughes LX display. Each molecule can rotate only around its long axis and has limited freedom of movement from side to side or up and down (Figure A-1a). The smectic LXs have a layered arrangment. The layers can slide over one another, because the molecules in each layer can move from side to side or forward and backward but not up and down. Within each layer, molecules may be ordered in ranks (Figure A-1b) or randomly distributed. The cholesteric, like the smectice, LXs consists of layers. Within each layer, however, the molecules are parallel, as are the nematic molecules. Molecules in one layer influence the layers above and below, so that the long axes of the molecules in these layers are displaced slightly and a helical pattern forms from layer to layer (Figure A-1c).

A very important property of liquid crystals is the dielectric anisotropy, $\Delta\epsilon$, a quantity used to describe the orientation of liquid crystal molecules in the presence of electric fields.

eq. A-1 $$\Delta\epsilon = \epsilon_{\parallel} - \epsilon_{\perp}$$

where:

$\epsilon_{\parallel}$ = dielectric permittivity in a direction parallel to the long axis of the LX molecule

$\epsilon_{\perp}$ = dielectric permittivity in a direction perpendicular to the long axis of the molecule

Eq A-1 describes the static dielectric behavior and is most useful in evaluating the molecular behavior of figure of merit for LX materials utilized for display purposes.

APPENDIX A

LIQUID CRYSTAL MATERIAL CHARACTERISTICS

5.5 Summary

This section presents a summary of the significant accomplishments in the design, fabrication, test, and assembly capabilities for the liquid crystal displays developed on this program:

- Interconnect techniques for high density display and integrated drivers.
- Low power, integrated drivers implemented which incorporate on-chip clocks, power-down circuitry, and few external signal connections.
- Development of the high value resistor processing technique.
- Fabrication of low-defect integrated drivers and defect-free active matrix arrays, with defect-free large area photomasks.
- Full characterization of high density displays and integrated drivers with automatic, computer-controlled equipment.
- Assembly and packaging techniques for high density displays (non functional) in an inexpensive, reliable package.
- Assembly of several defect-free 6 micron thick liquid crystal cells using nonfunctional, high density displays.
- Fabrication of a line defect-free medium density display, which was light sensitive.
- Implementation of a light block layer and intermediate dielectric material to solve the light sensitivity problem on the medium density displays.
- Full characterization of the medium density display and photomasks with automatic, computer-controlled equipment.
- Assembly and packaging techniques for medium density displays in an inexpensive, reliable package.
- Assembly of several non light sensitive, low-defect medium density displays.

The principal problems which remain on this program, and currently hinder the efforts to fabricate a high-contrast medium density display, are as follows:

- Further development of the smoothing techniques with polyimide films. These films require the appropriate application technique to become self-leveling; thus eliminating the mechanical polishing technique previously used on low density displays.

The current program funding had been exhausted before the smoothing techniques could be satisfactorily implemented.

driver circuits that are used in the demo-unit boards. Several functional, medium density displays were fabricated; unfortunately they exhibited the light sensitivity problem which was characteristic to all the other display assemblies and wafer lots fabricated on this program. After further process development the feasibility modules were finished through processing, assembly, and test on Hughes IR & D funds. These modules did not exhibit a light sensitivity, or "video wash out" problem.

In conclusion, the test and assembly capabilities were successfully demonstrated for both high and medium density displays. The implication for higher density displays with integrated drivers is that no significant problems are foreseen at this time for high density displays up to 50 p/mm. The testing and assembly techniques developed in this program would satisfactorily meet the requirements of these higher density displays. The medium density display assembly techniques for mounting the top pyrex plate and filling with liquid crystal, successfully demonstrated the extension of the similiar assembly techniques which were used on low density, large area LC/MOS displays.

5.4 Implications For Higher Density Arrays

The significant design and process accomplishments on this program have been previously discussed. In addition, the principal problems still to be overcome include:

- process development techniques for smoothing the display active area in order to improve its specularity and thus its brightness and contrast.

Once the above processing techniques were understood, the next anticipated set of hurdles for higher density display (50 p/mm), which incorporate integrated driver circuits, would include:

- development of processing techniques for silicon p-n junction with tighter geometries and higher breakdown voltages;
- development of optical lithography for large area displays with tighter geometries and intra-layer alignment restrictions.

These two areas would require significant technological advances to facilitate the design and fabrication of higher density active matrix displays with full 525 line TV resolution.

5.3 Status of Liquid Crystal Display Test and Assembly

A computer - controlled, automatic testing capability was developed and utilized on this program, for the complete characterization of the high and medium density displays and integrated drivers. In addition, the manual, microprobing capabilities of our test equipment were frequently utilized by engineering to diagnose and characterize the performance of the integrated driver circuits.

The Electroglas wafer probe station and the Matrix-switch module were utilized for photomask-related defect detection on the liquid crystal displays. Fortunately, the test results indicated there were no repeatable photomask-related defects which caused operational failures of either the display or driver circuits. The required system timing signals, shown in Figure 2-3, were generated by an Interface Technology Pattern Generator, and these signals were brought to the display through MOS/CCD driver modules. The relative ease of adjusting the signal timing and voltage levels provided the necessary flexibility for fully characterizing the integrated driver performance, despite the drain shift register design error.

Several nonfunctional, high density displays were assembled, which successfully demonstrated several new assembly and packaging techniques. For instance, each display was mounted first onto a molybdenum plate with an acceptable thermally-conductive epoxy. Next, the display assembly was mounted with epoxy coated mylar to the alumina substrate. This substrate provided easily accessible feed-thru pins on 0.10 inch centers for standard socket interconnection. The final package was rigid, inexpensive, compact, and easily manipulated during testing and final assembly. As a result of the integration of driver circuits, the alumina substrate required only 46 pins (actually 23 unique signals) to interface between the electronic boxes and the high density display. Unfortunately, the alumina substrate was larger than the volume specifications stated for this program. The assembly techniques for mounting the top pyrex plate and filling with liquid crystal demonstrated the integrity of a high density assembly with a 6 micron thick display cavity. The resulting uniform liquid crystal activation in the two assembled displays, demonstrated the extended assembly capability in the following areas:

- Tighter geometry registration in assembly;
- Concern for smaller particles in assembly; and
- Liquid crystal assembly over integrated driver circuitry

The thermal analysis study, reviewed in Appendix B, indicated that the integrated drivers would not adversely affect the liquid crystal as a result of their power dissipation.

The same computer-controlled testing equipment and Electroglas wafer probe station, previously described, were also used in testing the medium density display wafer lots. The devices, after wafer probing, are then assembled into displays and mounted onto the pyrex back plate which contains the gold interconnect lines. Next, the displays are wire-bonded and then activated by the demo-unit electronics boards. The electronics boxes built for this program were modelled after the hardware and discrete

- Chrome metal
- Aluminum
- Aluminum-silicon alloy
- Tapered metal etching
- Polysilicon-aluminum for step coverage

In general, these efforts did not produce consistently successful results. To pursue these approaches, or to develop new ones, significantly larger amounts of development efforts would be required.

Next, the intermediate dielectric material requires a low temperature deposition process so as not to cause metal migration through to the integrated driver circuits. This dielectric material should be compatible with semiconductor processing techniques, our liquid crystal material, and provide an optically flat surface over the active display area. The following process techniques and materials were investigated on this program for solving the intermediate dielectric problem:

- Chemical vapor deposited (450°C) silox
- Thin polyimide films (<.5 micron)
- Low temperature plasma deposited silicon nitride
- Sputtered deposited silicon nitride and silicon dioxide

In general, these efforts did not produce consistently successful results and significant continued developmental effort was called for.

In conclusion, the processing capability for fabricating high density displays which are not light sensitive was not developed on this program. The processing capability for fabricating integrated driver circuits was demonstrated on this program. To extend our processing capabilities for fabricating higher density displays, the aforementioned processing problems must first be solved (i.e., light blocking layer, intermediate dielectric layer, and display active area smoothing). Once these problems are resolved, the next higher density displays could approach 50 p/mm before lithographic limitations would become the critical problem. Processing capabilities currently exist at the Hughes Research Center in Carlsbad to fabricate CMOS devices with high density configurations and high p-n breakdown voltages. These characteristics are required in higher density displays.

The demonstration of a non light sensitive, functional medium density display illustrated our processing capabilities in fabricating LC/MOS displays. The development of a light blocking layer and intermediate dielectric material facilitated the solution of the light sensitivity problem initially exhibited by these displays. In addition, the approach to the dielectric material (a polyimide film several microns thick) lends itself to the implementation of "smoothing" on the medium density displays. The developmental efforts to implement a smoothing technique on the medium density displays, which is as optically flat as polishing the polysilicon layer on low density displays, is presently funded as a Hughes IR & D task. Further application of the accomplishments developed on this program, and in regards to smoothing the medium density displays, will be discussed in the summary section 5.5.

In conclusion, the interconnection of the high density display to its driver circuits was successfully demonstrated by integrating these drivers with the display on the same silicon wafer. The design fix to the drain driver shift register string was implemented on the last two wafer lots processed before the program redirection. These two wafer lots were not completed due to the redirection of the program. The principal reason for failing to demonstrate functional high density displays was attributed to the lack of an adequate insulator material between the light block material and top reflector electrodes in the display.

5.1.2 Medium Density Display

The interconnection of the medium density display with its discrete drivers was successfully demonstrated on this program. The present bonding equipment capabilities were used in wire bonding the .001 inch aluminum wire to the 100 micron square pads on the display interconnect lines.

One of the first medium density display assemblies, which was light sensitive, demonstrated a line defect-free display.

In conclusion, the operation of a medium density display (12.25 p/mm) was successfully demonstrated on this program. The incorporation of "smoothing" in the display active area to reduce random reflections from the underlying integrating circuit geometries was not fully implemented on this program, likewise the solution to the display light sensitivity problem was not achieved. These two activities were further supported and finally implemented on the medium density displays, with Hughes IR&D funding.

Although most of the medium density displays used in the four feasibility modules were not defect-free or "smoothed", these displays demonstrated Hughes' capability to design, fabricate and assemble a LC/MOS display with 12.25 pixel per millimeter pixel density for applications in projector and direct-view systems. Three of these feasibility modules were non - light sensitive over the active display array.

5.2 Status of Processing Capabilities

The demonstration of functional integrated driver circuits illustrated our processing capability to simultaneously fabricate these circuits with a high density display. The development of the high value resistors was successfully accomplished by altering the implant dose to compensate for the aluminum auto-doping effects.

However, there are several process techni ues which require further development efforts in order to successfully fabricate a functional high density display with integrated drivers. For instance, the light blocking layer requires an opaque material to prevent light from generating electron-hole pairs in the silicon substrate, adjacent to the boron diffused drain lines. This light block material must be conductive for use as the ground electrode of the vertical storage capacitor in each pixel. The following process techniques and materials were investigated on this program for solving the light blocking layer problem:

First, this section summarizes the high density display status just prior to the redirection of the program's objectives (and remaining resources) by the Tri Service Committee. The redirection options were outlined in a proposal by Hughes, which is described in Appendix C. Next, a summary is presented for the medium display status as to the present capabilities in fabrication and assembly. Finally, the present liquid crystal display design, fabrication, and assembly capabilities are extended to higher density displays and modular display packaging.

5.1 Status of the Liquid Crystal Display

5.1.1 High Density Display

The interconnection of the high density display with its integrated gate and drain drivers was successfully demonstrated on this program. Although the high density pixel design was not functionally demonstrated on this program, a successful miniature active matrix display was previously demonstrated for the Night Vision Labs, Ft. Belvoir, VA., using the same pixel cell design, without integrated drivers or the light blocking layer. However, the high density display developed for this program exhibited satisfactory electrical characteristics and low line defects in the active matrix array during characterization at the polysilicon layer test point. In fact, several active arrays were line defect-free at this test point.

The principle problems with the high density pixel display occurred with inter-layer shorting between the polysilicon interconnect to light blocking layer and to the top reflective electrode. In addition, the high density display design and photomask sequences prevented the implementation of smoothing the active array without significant efforts toward implementing a "self-leveling" film which would be compatible with current semiconductor processing techniques and our liquid crystal material.

The major circuit elements comprising the integrated drivers on the high density display were successfully demonstrated, as mentioned earlier. Several significant driver circuit concepts were demonstrated by the success with these integrated driver circuits. For instance, the drain driver video amplifiers demostrated a uniform output waveform over their 0.-20. volt range with only a +/- .25 volt variation. This amplifier performance is acceptable for uniformly driving the liquid crystal over the active array without incurring a striped or uneven video pattern, which might result from unmatched drain video amplifiers. Next, the gate driver circuits were powered-down during the video sampling period in a TV frame. This technique enabled the 240 gate driver shift registers to consume only 300 milliwatts of power, as predicted. Also, the drain driver circuits were powered-down during different portions of the TV frame time. For instance, when the 78 shift registers were not used for video sampling, they were powered-down. The 78 video amlifier circuits were likewise powered-down during the video sampling period, but were powered-up during the horizontal retrace period. Finally, the on-chip clocking circuits reduced the external timing circuits, external signal connections to the alumina substrate, and provided the display with functional options: full TV line interlace with a four display configuration, and alternate TV line sampling with non-interlace when using one display.

4.8.1 Discussion:

Several characteristics of dynamic scattering liquid crystal displays are pointed up by the data on three of the feasibility modules. In particular the angular dependence of the contrast is well understood in terms of liquid crystal properties. For any dynamic scattering liquid crystal display there will be an angle at which the contrast reverses. If the detector is aligned with the principle reflection of the lighting source then unactivated elements appear to be bright, since activated elements scatter some large fraction of the illumination away from the detector. If the detector is moved away from the principle reflection by an angle of about 30°, then the light reaching the detector is light scattered by the activated elements; unactivated elements appear dark, since they reflect (ideally) no light in the direction of the detector. At angles run 10-15° the amount of light scattered into the detector by activated elements is comparable to that reflected into the detector and thus the contrast is very poor.

The dependence of display contrast on wavelength is not due to the liquid crystal. Instead, it is due to the reflectivity of the Indium-Tin Oxide on the top plate electrode. Coatings which are uniformly reflective for a wide band of wavelengths are presently under evaluation, and if applicable will be incorporated into future displays.

The refresh rate dependence of the display's contrast is affected by both the liquid crystal conductivity and the storage capacity of each individual elemental capacitor. The liquid crystal is driven by a current flow which discharges the capacitor; the lower the refresh rate the lower the voltage on the capacitor (and hence on the metal electrode) drops before it is refreshed. The present material has been formulated for optimum performance with lower density displays which have a higher cell area ratio. It is adequate at 60 Hz rate; display of interlaced video would probably require that the dopant level in the liquid crystal be reduced, thus increasing the liquid crystal resistivity somewhat.

The variation of contrast with applied voltage is the effect which allows the display to render grey shades. It is noteworthy that the three displays evaluated agree so well as to grey shade rendition. This property is important to the performance of an optical quad consisting of four displays driven from a common video source, each providing one quarter of the displayed video image.

5.0 SUMMARY AND CONCLUSIONS

This section summarizes the significant accomplishments attained on this program, and reiterates the capabilities established for the design, fabrication, test and assembly of liquid crystal displays. In addition, the implications of the program accomplishments are discussed with respect to their application to optically-combined flat panel matrix displays and portable, direct-view flat panel display modules.

4-4 CONTRAST RATIO OF FEASIBILITY MODULES—REFRESH RATE DEPENDENCE

Contrast Ratio Refresh Rate Dependence			
Rate (Hz)	20/81-1	21/81-1	21/81-2
200	7.5	6.0	7.0
120	7.1	5.7	6.7
60	6.2	5.1	6.1
30	4.9	4.1	4.7

Measured in specular mode - 15° incident angle (Q)

4-5 CONTRAST RATIO OF FEASIBILITY MODULES—APPLIED VOLTAGE DEPENDENCE

Contrast Ratio Applied Voltage Dependence			
Vdrain(V)	20/81-1	21/81-1	21/81-2
25	9.6	8.8	9.1
20	8.6	8.3	8.3
15	7.5	7.2	7.0
10	5.0	4.9	4.8
5	1.6	2.0	2.0

Measured in specular mode - 15° incident angle

4-6 SPEED OF FEASIBILITY MODULES

Display Speed (msec)			
	20/81-1	21/81-1	21/81-2
Risetime	42	70	55
Falltime	260	520	390

Measured in specular mode - 15° incident angle

4-2 CONTRAST RATIO OF FEASIBILITY MODULES—WAVELENGTH DEPENDENCE

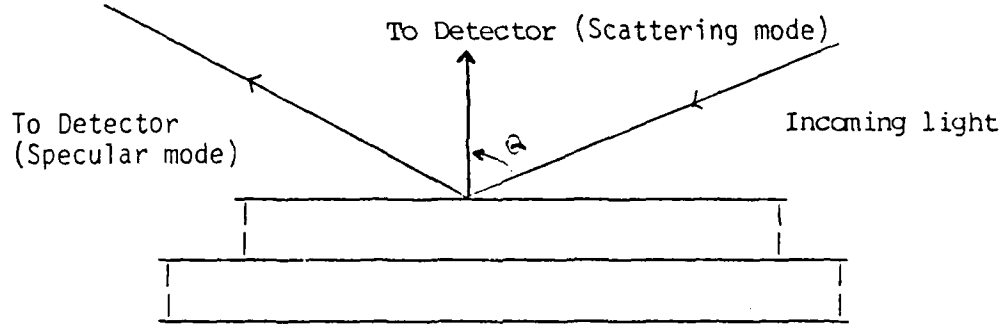
Contrast Ratio Wavelength Dependence			
inc(nm)	20/81-1	21/81-1	21/82-2
450	2.2	1.7	1.7
500	3.8	3.3	3.3
550	7.3	8.3	8.2
600	8.4	12.0	11.3
650	8.3	8.0	8.1
700	6.3	6.9	6.4

Measured in specular mode - 15° incident angle (Q)

4-3 CONTRAST RATIO OF FEASIBILITY MODULES—LIGHTING ANGLE DEPENDENCE

Contrast Ratio Lighting Angle Dependence			
Angle with normal, Q	20/81-1	21/81-1	21/81-2
10°		1.1	1.0
15°		2.0	1.5
20°		2.6	2.1
25°		4.3	4.5
30°		6.8	6.1
35°		7.4	6.0
40°		6.1	6.1
45°		5.5	7.2
50°		5.2	8.8

Measured in scattering mode



4.8 Evaluate and Deliver Feasibility Modules

Four displays were delivered as "Feasibility Modules" (FMs). Three of these units were not light sensitive but contained line defects; the fourth unit was light sensitive but line defect-free. All were filled with standard 2N-40 liquid crystal. Other information on these displays is summarized in Table 4-1.

Display Number	D'Lvd to	Light Sens.	Approx. No. Line Defects
43/80-1	AFAL	Yes	0
21/81-2	NADC	No	3
20/81-1	NVEOL	No	14
21/81-1	(Spare)	No	None before packaging; quite a few after packaging

More detailed measurements were made on three of the four modules. These include measurements of contrast ratio (as a function of either wavelength, lighting angle, refresh rate, or applied voltage), rise time, and fall time. These data are summarized in Tables 4-2 - 4-6.

DSM can be activated by either AC or DC signals. When AC is used, the frequencies are typically less than 1 KHz. The voltage value is dependent upon the material constituency and classification and ranges from

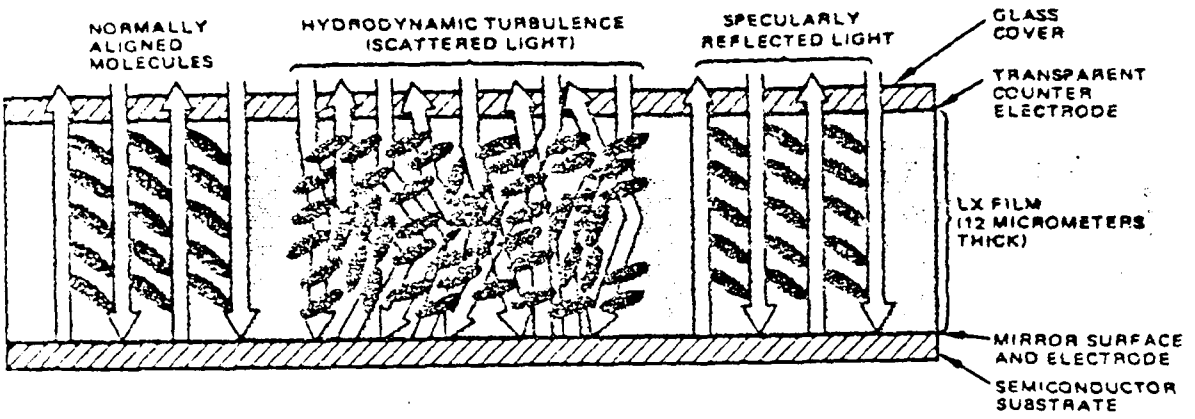


Figure A-2 Nematic LX shown in dynamic scattering mode (DSM)

0.5 volt to 60 volts. In the Hughes LX matrix display, the excitation is unipolar and of varying amplitude (22 volts or less) depending upon video scene content. An AC bias of 60 volts peak to peak amplitude and appropriate frequency (depending upon material consitiuency) can be used to help return the molecules to their normally aligned state after the excitation is removed.

A.1.2 Field Effects

Another way to take advantage of the sympathetic alignment and the optical anisotropy of nematics is the twisted nematic configuration shown in Figure A-3. The design of the twisted nematic cell is the same as for the DSM, except that the cell walls are treated to make long axes of the LXs parallel to the plane of the cell wall. As a result, on each cell wall the long axes of the LX molecules are parallel to each other as well as to the plane of the cell wall. The cell is assembled to form an angle of 90° between the direction on the other wall. Calculations show that the orientation of the long axes of the molecules varies smoothly across the cell thickness from one orientation to the other. Hence, the name twisted nematic.

If light incident on the cell is plane polarized either along the direction parallel to the long molecular axis or perpendicular to it, the plane of polarization of the light emerging from the other side of the LX cell is rotated 90°.

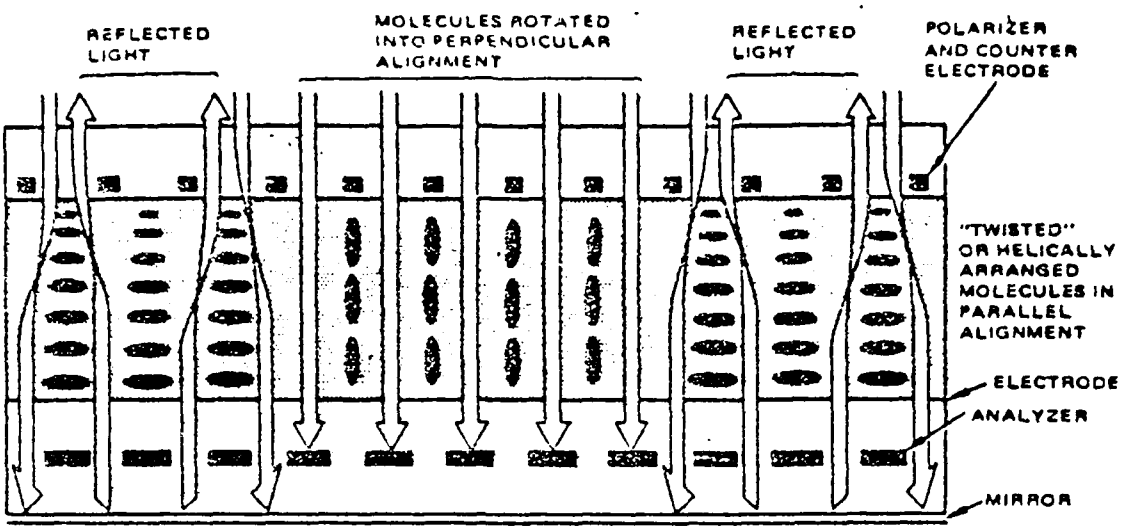


Figure A-3. Twisted Nematic LX shown in field effect mode.

When viewed through a polarizer oriented normal to the analyzer, this emerging light is observed to pass through the polarizer. However, if a field of sufficient strength (typically a few volts) is applied to the cell, light is blocked by the analyzer. The reason is that the molecules in the bulk change their alignment with the cell wall from parallel to perpendicular. As a result, no rotation of the plane of polarization of the light occurs when the field is applied. Since the analyzer is aligned normal to the polarizer, light is now blocked. Thus, by using a linear polarizer and analyzer in conjunction with a twisted nematic configuration, the intesity of the transmitted (polarized) light can be modulated with an electric field; hence the term "field effect", as opposed to DSM which is a current induced effect.

In their present state of development, nematic materials operated in the dynamic scattering mode, offer the most promising application to the matrix display technique described in this report. However field effect operation would be equally desirable if there were a practical method of applying a polarizer to the reflective surface of the matrix display substrate.

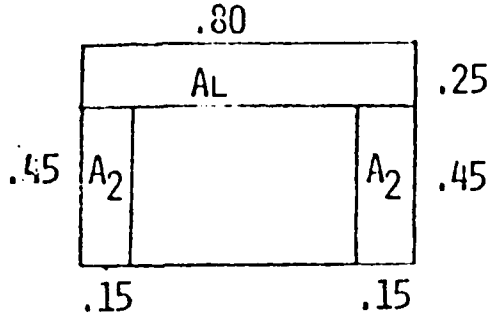
APPENDIX B

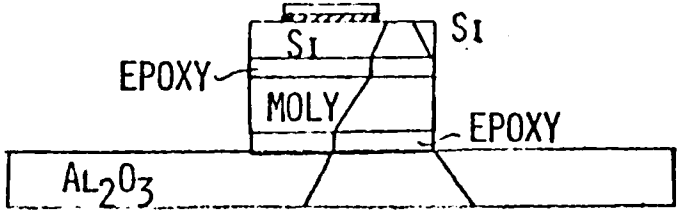
THERMAL ANALYSIS OF HIGH DENSITY DISPLAY PACKAGE

THERMAL ANALYSIS OF H403[illegible]

SWEEP DRIVERS

HUGHES





SILICON .028 THICK

AREA SWEEP DRIVERS $A_2 = (.45 - .014)(.15 - .014) = .059$ IN^2

AREA VIDEO DRIVERS $A_1 = (.80 - .014)(.25 - .014) = .185$ IN^2

$$\theta_{SI-E} = \frac{.028}{3.3(.45)(.15)} = .14 \text{ °C/WATT}$$

$$\theta_{E-MOLY} = \frac{.002}{(.009)(.464)(.164)} = 3 \text{ °C/WATT}$$

$$\theta_{MOLY-E} = \frac{.050}{3.4(.489)(.189)} = .14 \text{ °C/WATT}$$

$$\theta_{E-AL_2O_3} = \frac{.002}{(.009)(.514)(.214)} = 2.02 \text{ °C/WATT}$$

$$\theta_{AL_2O_3} = \frac{.040}{(.85)(.554)(.254)} = .33 \text{ °C/WATT}$$

TOTAL THERMAL RESISTANCE

$\cong$ 5.6 °C/WATT

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THERMAL ANALYSIS OF H4035
VIDEO DRIVERS

HUGHES

$$\theta_{Si\text{-}E} = \frac{.028}{3.3(.8)(.25)} = .04\ ^\circ C/WATT$$

$$\theta_{E\text{-}Moly} = \frac{.002}{(.009)(.814)(.264)} = 1.03\ ^\circ C/WATT$$

$$\theta_{Moly\text{-}E} = \frac{.050}{3.4(.864)(.314)} = .05\ ^\circ C/WATT$$

$$\theta_{E\text{-}Al_2O_3} = \frac{.002}{(.009)(.914)(.364)} = .77\ ^\circ C/WATT$$

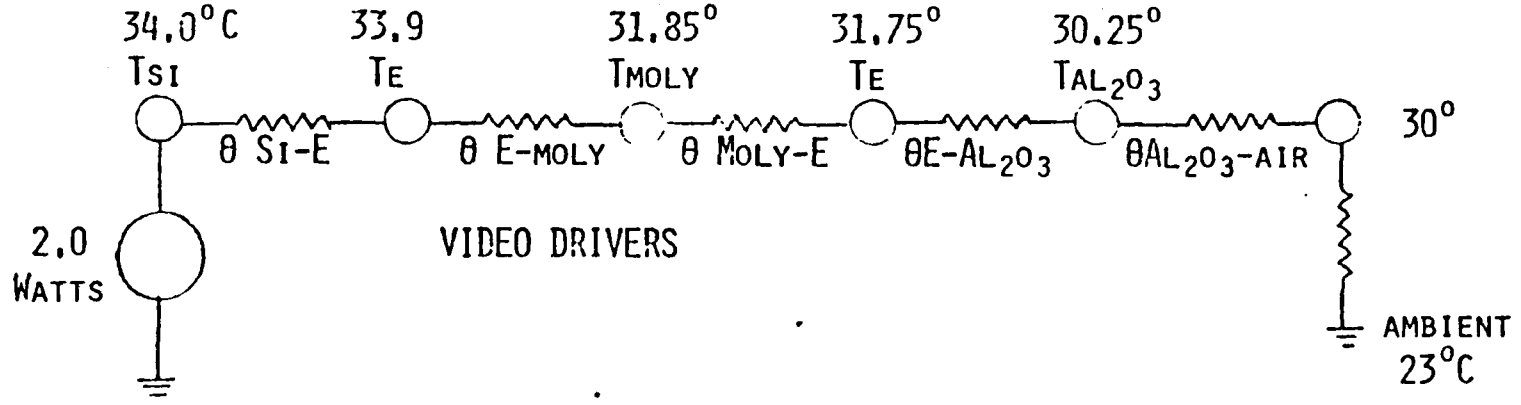
$$\theta_{Al_2O_3} = \frac{.040}{(.85)(.954)(.404)} = .12\ ^\circ C/WATT$$

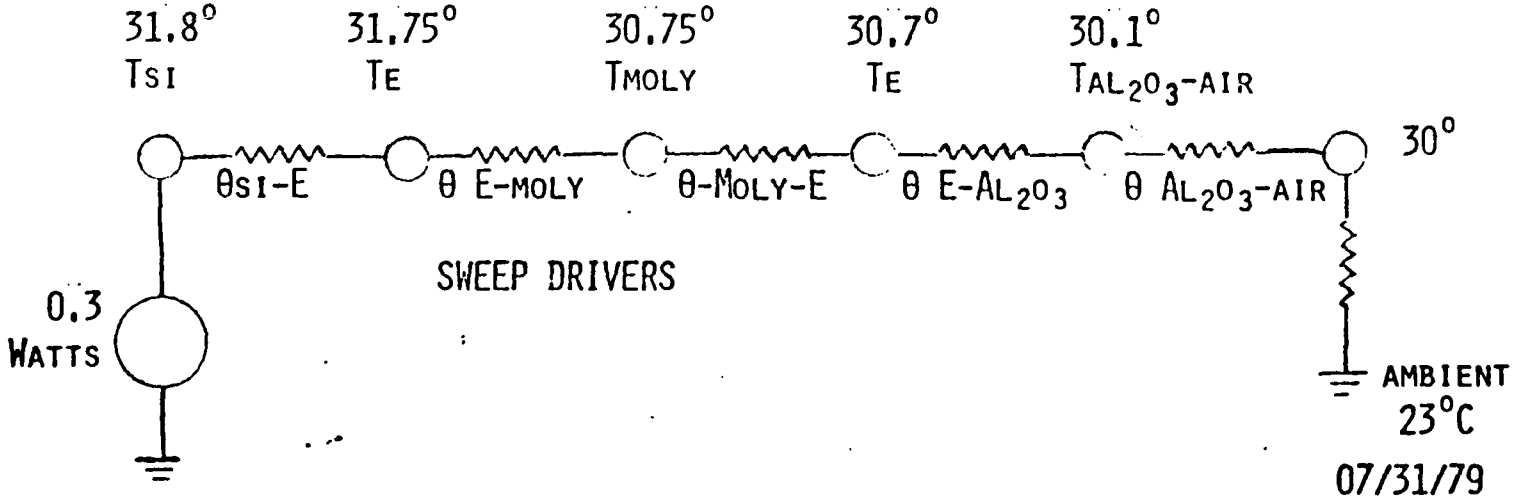
TOTAL THERMAL RESISTANCE $\simeq$ 2 °C/WATT

07/31/79

THERMAL EQUIVALENCY SCHEMATIC MODEL

HUGHES





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APPENDIX C

PROPOSED APPROACH CHANGE ON THE LC/MOS HIGH-DENSITY PROGRAM

INTRODUCTION

This submittal is a proposal change to the Liquid Crystal Metal-Oxide Semi-Conductor (LC/MOS) High-Density Program under development for the Army Night Vision and Electro-Optical Laboratories, Ft. Belvoir, VA. This change is recommended to achieve a deliverable higher density (greater than 100 ppi) display unit within the allocated budget.

The LC/MOS High Density Program was begun in October 1978 with the ambitious goal of developing a 240 by 312 picture element (pixel) liquid crystal matrix display with fully integrated drive circuitry. The proposed design called for a single 0.75 by 0.87-inch silicon chip containing the 588-pixel/inch display surface and the 10,000 additional transistors to drive the display with an input from a standard serial television signal source. The design deviated from that used for the previous density (100-pixel/inch) liquid crystal matrix displays in that a vertical multiple-plate capacitor structure was substitued for the simple horizontal two-plate capacitor structure used in the previous designs. The vertical structure makes it possible to provide the required storage capacitance within a very small area without pushing the guidelines for photolithographically controlled masking and etching. Unfortunately, it requires that a capacitor plate or one of the dielectric layers also be a lightblocking layer so as to prevent photon-excited carriers from interfering with the operation of the underlyinng transistors that form the addressing circuits.

The key technical challenges on the high-density display program have been the development of: (1) a stable horizontal resistor for assuring linear operation of the on-chip drive circuits; (2) a suitable light-blocking layer for protection of the addressing circuits underlying the active display area; and (3) a compatible processing procedure for display surface and display driver fabrication. Success in the first area was achieved by controlling the resistivity of a doped polysilicon layer to the tolerances required for the linear drive circuitry. However, no acceptable solution has yet been found for the light-blocking layer. The original plan called for using aluminum as the light-blocking layer and for using a dielectric material deposited at a low temperature as the overcoating insulator. Unfortunately, attemps to use the low-temperature dielectric have not been successful. Moreover, prelinimary work on developing a smoothing technique for existing displays has recetly shown that the best smoothing technique also requires compatibility with high temperature processing. As a result of the problem with the light-blocking layer, Hughes is proposing the following changes in the program. These changes are predicated on anticipated future applications as well as existing capabilities. They utilize existing techniques to fulfill future requirements.

The majority of future applications are expected to require a medium-density display. Interfacing to the display with miniature cabling will no longer be possible. Drive circuitry will have to move onto a common carrier with the display to achieve interconnection. One can integrate display and drivers, as is the case now, or leave them separate, connecting them by use of existing wire-bonding technology. Integration, as indicated, requires significant process development. Wire-bonding

of the display and drivers (that use existing processing) is therefore the remaining choice. It will be compatible with optical combination or modular concepts to meet display requirements. The approach will commence with a bonding study to determine the upper limit on bonding density from presently available bonding equipment. The results of this study will be discussed in a design review on the proposed medium-density 12.55 p/mm (312 pixels per inch) in a 200 by 288 pixel configuration. The bonding study results will confirm our present design rule assumptions on bond pad spacing limitations. These results will be incorporated into this display layout.

The medium-density display will be fabricated with a fully developed sevenmas. MOS process. There will be four displays on a three-inch wafer. Wafer processing will include six wafer lots, containing twenty wafers, with additional two wafer lots for driver circuits. These wafer lots will provide the program with four deliverable displays that exhibit the state-of-the-art in display quality and three sets of driver circuits to drive 175 by 175 display lines. Our existing smoothing process sequence will be incorporated on the six display wafer lots.

A new circuit plate design will be generated to allow driving the display lines with the existing set of interconnect cables and driver boards. However, the cables will only allow a display sector of 175 by 175 pixels to be activated. The definition of which 175 display lines are to be bonded on the medium-density display and how redundant drive will be implemented will be discussed in the design review involving the Hughes design group and the Tri-Service program monitor.

At present, an electronics demonstration box is utilizing copies of the IHUD driver boards, driver circuits, and kapton interconnect cables. This electronics box design will be duplicated for delivery of two drive boxes and one set of spare drive boards and cables.

1. Description of the Deliverables-(Reference Paragraph 3.0 of Attachment 1) Hughes proposes to deliver four feasiblity modules (FM), two electronics boxes, and one set of spare interface cables, driver circuits and boards. The feasiblity modules will accept standard 525-line, 30-fps composite TV. The displays will be fabricated with the present seven-mask MOS process on three-inch wafers, allowing four displays per wafer. It is anticipated that the rectangluar display layout will have 200 gate lines and 288 drain lines and will provide for driving both ends of the same display line. The MOS fabrication of these medium-density-displays will incorporate smoothing techniques to reduce reflections from the circuit irregularities. Our purpose is to provide a means of assessing the importance of smoothing relative to high-density displays.

   Smoothing enhances liquid crystal display contrast and image quality by reducing random reflections caused by surface irregualrities. At its present level of development, smoothing techniques reduce these reflections from between the underlying MOS capacitor and the top reflective electrode. VIA elimination is the subject of future work and will not be part of this task.

2. Feasibility Module Design Requirements and Goals (Reference Paragraph 3.2 of Attachment)

2.1 (Reference 3.1.1) Pixel Density (p/mm) 12.25
2.2 (Reference 3.1.2) Format
(1) Vertical Pixels (#) 200
(2) Horizontal Pixels (#) 288
2.3 (Reference 3.1.4) Electronics
Two electronics boxes will be delivered on this program. They will include the driver circuits, boards, and kapton cables for interfacing with the medium-density display. An additional set of spare driver circuits, boards and cables will also be supplied as backup to the electronics boxes. The electronics boxes will accept 525 line composite TV and provide the video signal to the liquid crystal display module via the kapton cables. Both electronics boxes are extensions of a demonstration display unit Hughes presently uses and require duplicating the boards and electronics units.

3. Bonding Study

An additional task is proposed in this program to implement the medium density display concept with the existing set of driver boards and kapton cables. The purpose is to establish the upper limit of bonding density between two adjacent metal-oxide semiconductor (MOS) circuits. The approach will be to evaluate the maximum bond density of available equipment in terms of: accuracy of bond placement; lead dress; compatibility with display assembly procedures; and bond reliability. After preliminary tests on simple metalized surfaces, masks will be generated and staggered metal stripes patterned on MOS circuits to simulate actual bonding conditions. Once an upper limit for bonding density has been established, the bonds themselves will be evaluated on the basis of their ability to meet MIL-STD-883 requirements. With the results of this bonding study in hand, future plans are possible regarding peripheral drivers that interface with the display on a common carrier. However, the reality of the present is to design a circuit plate to interface existing cables and driver electronics with the medium-density display.

4. Statement of Work

Task 1. Bonding Study

The purpose is to establish the upper limit of bonding density between two adjacent MOS circuits. The bonds will be evaluated on the basis of their ability to meet MIL-STD-883 requirements. The bonding study will be concluded within the first two months of the program. A report of the findings will be submitted in the Task 3 Design Review.

Task 2. Display Design

The purpose is to establish a medium-density liquid crystal display of 200 by 288 pixels. The display will be fabricated with our fully developed seven-mask MOS process. There will be four display patterns per three-inch wafer. The availability of redundantly driving the display lines will be provided for, pending the incorporation of the bonding study results of Task 1.

Task 3. Design Review

This review will include the Tri Service monitor and the Hughes design team in liquid crystal displays. Results of the bonding study will be presented in a report, along with the implications to peripheral driver circuit techniques. The design of the medium-density liquid crystal display will be discussed. A decision on the go-ahead to order the display photomasks will be jointly made. Also, it will be decided which area in the display a 175 by 175 pixel sector shall be bonded out to the existing interconnect cables. This design review will occur at the end of the second program month.

Task 4. Circuit Plate Design

The purpose is to establish a pyrex circuit plate design that allows interfacing the medium-density liquid crystal display to the existing set of interconnect cables. The design and fabrication of twenty circuits plates will be completed by the fourth month in the program.

Task 5. Redesign (Option)

In the event of a design error or defect in the photomask procedure, a redesign of a few photomasks may be required to develop working displays of high quality and adequate yield. This task will be decided after evaluation of the first few wafer lots upon completion of the MOS processing procedure.

Task 6. Wafer Production

After the initial runs of wafers have been thoroughly evaluated and process limits determined, wafers will be processed and tested to obtain display circuits to be used in the feasibility modules. Lots of 20 wafers will be run approximately once a month for 8 months.

Task 7. Assembly of Four Feasibility Modules

The assembly techniques developed previously will be applied to the construction of deliverable displays, to interfacing the display with the separately evaluated signal processing electronics, and to fabricating module display systems. The four feasibility modules will be delivered in the tenth month of the program, or sooner as availability dictates.

Task 8. Assembly and Delivery of Two Electronics Boxes

This task will consist of the design and fabrication of the peripheral electronics themselves (including incoming signal stripping and multiplexing), and the fabrication and packaging of the display system. The displays will be assembled with a flat pyrex top plate. No incorporation of lighting into the system will be introduced other than ambient room lighting. The display will be mounted for direct view non-light trapped. The assembly and delivery of the two electronics boxes will occur in the tenth month of the program, or sooner as availability dictates.

Task 9. Assembly of One Set of Spare Drive Electronics Boards

This task will be the assembly of spare driver boards and interconnect cables as backups to the two electronics boxes in Task 8. These spare items will be delivered in the tenth month.

Task 10. Submittal of Final Report

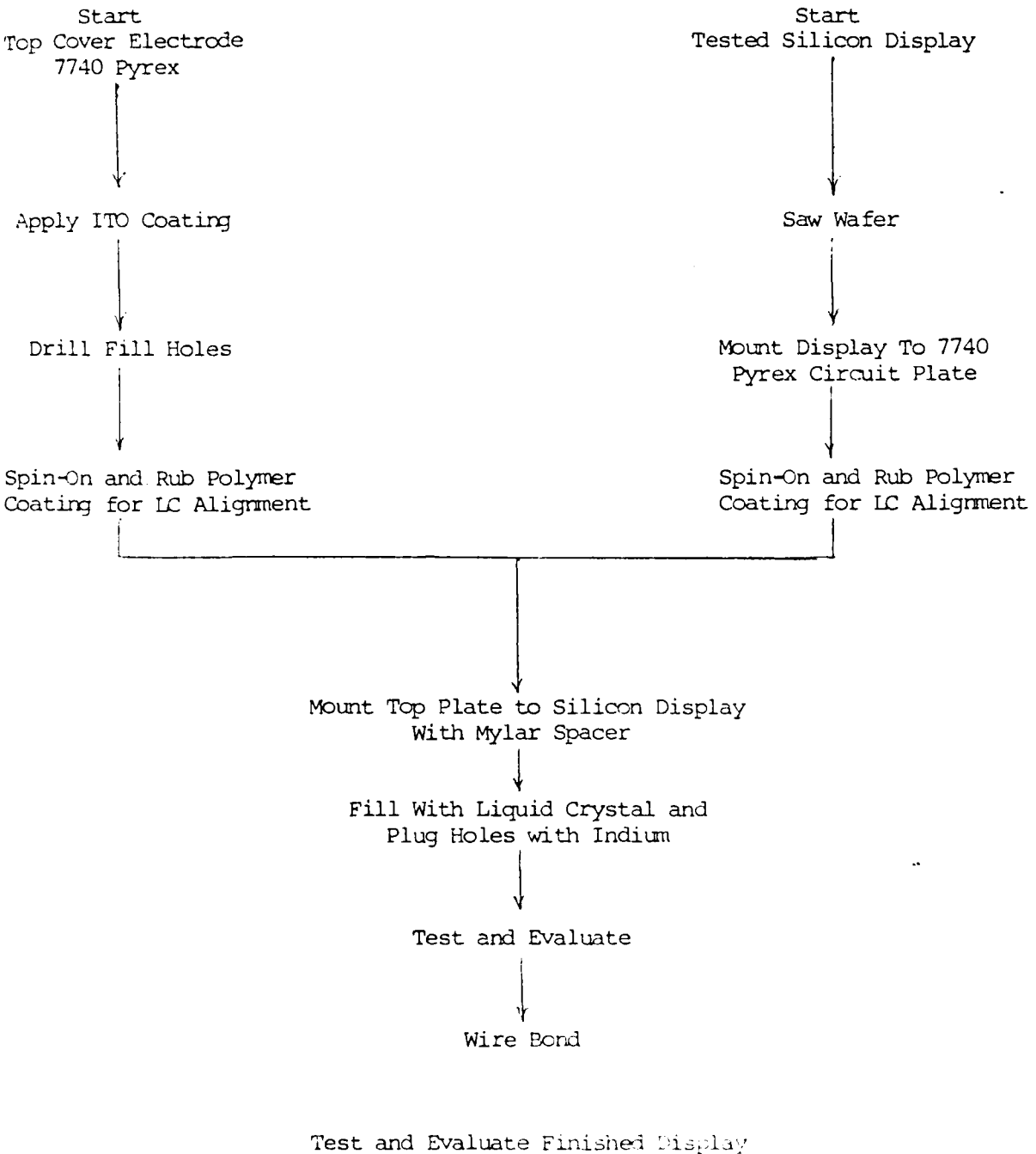
This report will summarize the MOS processing and assembly techniques and results on this program. Implications for future applications of this medium-density display will be entertained with peripheral driver circuitry techniques for driving the display. A review of new insights into further extensions of the present technology will also be discussed. This report will be submitted in the tenth month of the program.

5. Program Milestones

An extension in the present program milestones is requested based on the incorporation of the smoothing of the liquid crystal displays, the bonding study and necessity to design a medium-density display and circuit plate and acquire photographic masks for fabrication in the MOS processing facility. The necessity of concluding the bonding study before the liquid crystal display photomasks are finalized requires these operations to be done serially. The wafer lot processing will require five months to process eight wafer lots. The first display available for assembly and testing will occur in the sixth month of the program go ahead. Included in this processing cycle will be the smoothing sequences to reduce the reflections and enhance the display contrast and image quality. Because these processes and assembly steps must be done in a sequence, a ten-month extension on the present program milestones is required. Hughes will perform the tasks in this program change within the remaining budget allocation. With this time extension, Hughes will be able to deliver the aforementioned four deliveries with smoothing performed on the liquid crystal displays.

APPENDIX D

ASSEMBLY FLOW CHART FOR THE MEDIUM DENSITY DISPLAY


Start
Top Cover Electrode
7740 Pyrex
Apply ITO Coating
Drill Fill Holes
Spin-On and Rub Polymer
Coating for LC Alignment
Start
Tested Silicon Display
Saw Wafer
Mount Display To 7740
Pyrex Circuit Plate
Spin-On and Rub Polymer
Coating for LC Alignment
Mount Top Plate to Silicon Display
With Mylar Spacer
Fill With Liquid Crystal and
Plug Holes with Indium
Test and Evaluate
Wire Bond
Test and Evaluate Finished Display

END